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Handbook for

RECEIVER, RADIO FREQUENCY

5820-99-519-7019

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ANY SUGGESTIONS FOR AMENDMENTS OR ADDITIONS TO THIS BOOK SHOULD BE SUBMITTED TO THE DIRECTOR GENERAL, WEAPONS (NAVAL) THROUGH THE USUAL CHANNELS FOR ONWARD TRANSMISSION TO DWRDS.

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FOREWORD

This book uses Part 5 only of the NWS 1 seven-part documentation format. Associated system or equipment information is given in:-

(a) BR 4144 - Handbook for Transmit Receive Equipment Type 641.

(b) BR 4218 - Handbook for Receiver Outfit CJM.

(c) BR 4219 - Handbook for Transmitter Drive Outfit TDC.

COMPLETE LIST OF HANDBOOKS

FOR TYPE 641 AND ASSOCIATED EQUIPMENT

BR 4144(2)		WIRELESS TRANSMITTER/RECEIVER TYPE 641 - USER HANDBOOK
BR 4144(3 & 4)		TYPE 641 TRANSMIT-RECEIVE EQUIPMENT
BR 4144(6)		TRANSMIT-RECEIVE OUTFIT TYPE 641 - ACCEPTANCE TRIALS
BR 4145	Vol 1	MODULATOR TUNING UNIT 5820-99-519-6983
BR 4145	Vol 2	MODULATOR TUNING UNIT 5820-99-519-6983
BR 4146		SYNTHESIZER, ELECTRICAL FREQUENCY 5820-99-519-7000
BR 4147	Vol 1	RECEIVER, RADIO FREQUENCY 5820-99-519-7019
BR 4147	Vol 2	RECEIVER, RADIO FREQUENCY 5820-99-519-7019
BR 4148	Vol 1	100 WATT SELF-TUNING AMPLIFIER AND ANTENNA MATCHING UNIT
BR 4148	Vol 2	100 WATT SELF-TUNING AMPLIFIER AND ANTENNA MATCHING UNIT
BR 4218		RECEIVER OUTFIT CJM
BR 4219		TRANSMITTER DRIVE OUTFIT TDC

RECEIVER, RADIO FREQUENCY

5820-99-519-7019

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CHAPTER 1

GENERAL DESCRIPTION

Introduction

Figure 1.1

1. Receiver, Radio Frequency 5820-99-519-7019 is the automatically tuned, independent sideband receiver used in Transmit Receive Equipment Type 641 and Receiver Outfit CJM.

2. It will receive ssb, dsb, mcw, cw and fst signals in the frequency range 240 to 525 kHz and 1.0 to 27.9999 MHz. Antenna input circuits include automatic protection against large r.f. voltages.

3. Two stages of amplification using valves and six automatically tuned circuits precede the first frequency change which produces an i.f. of 4 MHz or 1 MHz, for frequencies above or below 8 MHz. The 4 MHz i.f. is amplified and subjected to a second frequency change to produce an i.f. of 1 MHz. The amplified 1 MHz i.f., from the band above or below 8 MHz, is again mixed to produce a final i.f. of 100 kHz.

4. The output from the associated Synthesiser at its indicated frequency is inhibited. The three signals which would have been combined to form it are mixed in a Frequency Offset Unit to provide the local oscillation for each frequency change. Two automatically tuned circuits are used to filter the first oscillator frequency, and for speech clarification the synthesised input for the final i.f. may be replaced by one from a manually controlled oscillator.

5. The final i.f. at 100 kHz is supplied to two receiver channels via crystal filters. One channel is used for usb, dsb and the other for lsb reception. In each channel there are four stages of i.f. amplification all subject to A.G.C., the time constants for which are varied with the type of reception set.

6. Demodulation is effected by an envelope detector for dsb reception and by balanced modulators for ssb reception. The amplified audio output from each channel can be switched to a built in loudspeaker or monitored by headphones at one of three Receiver outputs, one local and two remote.

7. The class of reception is selected by front panel system switches which control diode switches to select the appropriate circuits.

8. For automatic tuning purposes the r.f. tuning circuits are disposed into six frequency ranges. The circuits for the appropriate range are automatically selected by a Ledex motor system which is positioned by setting the MHz control on the associated Synthesiser. The circuits thus selected are then servo tuned to the required frequency, the servo reference voltage being determined by the positions of the MHz and the 100, 10 and 1 kHz controls.

Physical Description

Figures 1.2, 1.3

9. The Receiver is a drawer unit, carried on runners, comprising the sub-assemblies listed in Table 1.1. Each sub-assembly or unit is numbered as shown to assist in component location. Where alternative descriptions are given the second is the NATO Stock one.

NOTE: Items marked * - 5A, 7A, 8A and 9A are used in Link 11 operation of the Receiver. Full details are given in Chapters 14A, 15A and 16A.

Table 1.1 Component Location Coding

UNIT	DESCRIPTION	NSN
1	Chassis and Front Panel Assembly	
2	Tuning Unit Receiver	5820-99-519-7020
3	Frequency Offset Unit	5820-99-519-7027
4	Panel Servo Supply	5820-99-519-6986
5	Amplifier Audio Frequency	5820-99-519-7030
*5A	Amplifier Audio Frequency	5820-99-758-9180
6	Panel Receiver Auxiliary Circuits	5820-99-519-7032
7	Panel Demodulator	5820-99-519-7029
*7A	Panel Demodulator	5820-99-758-9179
8	Panel Automatic Gain Control } usb	5820-99-519-7028
*8A	Panel Automatic Gain Control } usb	5820-99-758-9181
9	Panel Automatic Gain Control } lsb	5820-99-519-7028
*9A	Panel Automatic Gain Control } lsb	5820-99-758-9181
10	Amplifier Intermediate Frequency usb	5820-99-519-7031
11	Amplifier Intermediate Frequency lsb	5820-99-519-7031
12	Panel Filter Switching	5820-99-519-7023
13	Crystal Filter Assembly	
14	Power Supply	5820-99-519-7022
15	Stabiliser Board	5820-99-521-9421
16	Stabiliser Board	5820-99-521-9422
17	Diode Board DB2	
18	Diode Board DB1	
19	4 MHz I.F. Board or Amplifier I.F.	5820-99-521-9418
20	1 MHz I.F. Board or Amplifier I.F.	5820-99-521-9416
21	First Frequency Changer Board or Panel Electronic	5998-99-016-0633
22	100 kHz Oscillator Board or Oscillator A.F.	5820-99-521-9420
23	1.1 MHz and 3 MHz Amplifier Board or Panel Electronic Circuit	5820-99-521-9419
24	F.O.S.U. Wideband Amplifier	
25	1 MHz Limiter Board	

10. Units 2, 3, 13, 14 are separate sub-chassis connected by coaxial plugs and sockets and fastened to unit 1 by screws.

11. Units 4 to 12 are printed wiring boards with edge connectors which plug into sockets on unit 1. Functionally, units 8(8A) and 10 are for usb/dsb operation, units 9(9A) and 11 for lsb operation.

12. Units 15, 16 are functionally part of unit 14. They are plug in printed wiring boards retained by clamp plates. Their associated control transistors VT2, VT3 are mounted, with heat sinks, on the parent cabinet.

13. Units 17, 18 are associated with switching circuits. They are printed wiring boards with soldered connections.

14. Units 19 to 25 are printed wiring boards, functionally part of unit 2. Units 19 to 23 plug into sockets. Units 24, 25 are connected by coaxial plugs and sockets and by soldered terminals.

15. Two extension panels are provided so that plug-in boards can be tested while the equipment is operating.

16. The front panel contains fuses, controls, indicators and a loudspeaker as shown in Table 1.2. It hinges down for access to the associated components, including Ledex protection relay 1RLB.

24. In the R.F. Input Filter Assembly the r.f. input from 2RLA1 is coupled to the first of three inductors which, with main tuning capacitors 2C17, 2C19, 2C27 form three coupled tuned circuits. They afford front end protection and provide a voltage gain of 8 or 9 dB to an on-tune signal and an attenuation, relative to this, of about 30 dB to signals 5% off-tune.

25. The output from the r.f. input filter is fed to the grid of the first valve in the R.F. Amplifier Assembly. The circuit between the two pentodes used in the amplifier is tuned by main tuning capacitor 2C57. At $2\frac{1}{2}$% off-tune, this tuned circuit provides enough attenuation to reduce grid to grid gain to less than unity, except on range 1 for which the selectivity is reduced. An A.G.C. voltage which is produced from the combined outputs of Panels Automatic Gain Control, units 8 and 9, is applied to both stages. The fast acting A.G.C. has attack and decay time constants of about 1 millisecond.

26. The anode load of the second valve in the R.F. Amplifier is the coupling winding of a coupled pair of tuned circuits in the Oscillator Filter Assembly. These circuits are tuned by main tuning capacitors 2C71, 2C73 and form an r.f. filter which, with the tuned circuit in the r.f. amplifier, gives the required pass-band response.

Automatic Tuning

27. In the associated Synthesiser a switch wafer on the MHz decade control shaft applies -41 V to one of the plugs 2PLAC-C, D, E, F, H, J. This completes, via 2SA2F, the circuit from +41 V for Ledex rotary solenoid 2SA. The solenoid operates until 2SA2F isolates the live plug. Other switch wafers driven by 2SA have then selected the band-pass filters required for tuning to the frequency set on the Synthesiser. (One switch wafer, 2SA2B, is used in Type 641 to change the range control voltage from -41 V to -30 V and switch it to the Modulator Tuning Unit. 2SA2B is not used in Outfit CJM.)

28. The main tuning capacitors are driven by the 400 Hz, two-phase servo motor 2X1 which is controlled by Panel Servo Supply, unit 4. The output of a 400 Hz Wien Bridge oscillator in unit 4 is split and amplified to provide a push-pull output to the reference phase winding of 2X1 and, via a 90% phase shifter, to a chopper modulator.

29. 2X1 also drives the slider of a 10-turn helical potentiometer 2RV1 which is connected across 30 V. The d.c. voltage tapped from 2RV1 thus represents the position of the tuning capacitors, and provides one d.c. input to unit 4.

30. A d.c. voltage from about 0.75 V to 28 V at 1PLAA-L represents the positions of the Synthesiser decade controls and provides the other d.c. input to unit 4.

31. The voltage level and polarity of the resultant d.c. input to the chopper modulator determines the amplitude and phase of the a.c. output from the servo amplifier which supplies the control phase of 2X1, so that it rotates in a direction to reduce the d.c. input. The input level to the chopper is limited and a phase advance circuit prevents hunting. 2X1 drives the tuning capacitors until the voltage from RV1 is equal to that at 1PLAA-L, when there is no d.c. input to unit 4 and the filters are tuned to the frequency set on the Synthesiser.

32. Interlock circuits. The 400 Hz oscillator and the control phase amplifier in unit 4 depend on supplies of -30 V and -22 V respectively. These "during tune" supplies are switched by triggering circuits in Panel Receiver Auxiliary Circuits, unit 6, so that they are applied only while tuning is taking place.

RADIO FREQUENCY INPUT

Figures 1.6, 1.9

Overload Protection

17. The r.f. input from the antenna at 2PLAD is connected via the R.F. Input Filter Assembly to 2 PLAL. When the Receiver is switched on 2RLA is energised, 2RLA1 makes to connect a coupling winding between 2PLAD and 2PLAL, and 2RLA2 makes. The r.f. input from 2RLA1 is also taken to the Overload Prevention Board where a fraction of the voltage which appears across the coupling winding is applied to an overload detector and bistable circuit which controls 2RLA. If the voltage applied to the detector exceeds about 5 V the bistable is triggered to de-energise 2RLA.

18. The input winding will carry 0.5 A without damage but off-tune the input impedance is low and a high r.f. input voltage could cause excessive current to flow without operating the overload protection circuit. For this reason the protection arrangements for common antenna working are different from those for only one Receiver.

19. Common antenna working. 2PLAL provides the aerial output to another Receiver. As the feeder cable is finally terminated in 75 ohms off-tune antenna voltages to produce more than 0.5 A are most unlikely. Protection is provided, therefore, only against high voltages on-tune. Terminals B, C and A, C are linked so that when 2RLA is de-energised 2RLA1 provides a direct antenna connection to 2 PLAL via B, C.

20. Single antenna, single receiver working. B, C and A, C are not linked. Protection against high input voltages off-tune is provided by fitting a short-circuited terminating socket to 2PLAL and inserting a 12 ohm resistor in series with the coupling coil. The voltage developed across the resistor will operate the overload protection circuit before the current through the coupling coil reaches 0.5 A. If the Receiver is required to operate with high level signals off-tune the short circuit must be replaced by a terminating resistor which, with the series resistor, will limit the current to 0.5 A at the maximum input signal level required. When 2RLA is de-energised 2RLA1 breaks to disconnect the antenna.

21. In both arrangements, when 2RLA is de-energised 2RLA2 changes over to switch on the CUTOUT indicating lamp and to mute the receiver by allowing Diode Board DB2, Unit 17, to switch -30 V to Panel Automatic Gain Control, unit 8 or 9.

22. The Overload Prevention Board must be reset manually by switching the Receiver supply OFF and ON again. During simplex operation it is reset automatically on RECEIVE by the removal of -30 V from the overload bistable.

R.F. Stages

23. There are six sets of band-pass filters for tuning, one for each frequency range. The set for a particular range is automatically selected by the position of the MHz control on the associated Synthesiser, using Ledex driven switch wafers. In each set thus selected there are eight tuned circuits, six for the r.f. stages and two for the local oscillator frequency. These circuits are automatically tuned to the frequency set on the Synthesiser by eight servo-driven variable capacitors which are ganged together. The same main tuning capacitors are used on every range.

43. To avoid spurious response problems the normal output of the Synthesiser is inhibited and its component frequencies are mixed in the Frequency Offset Unit, unit 3, where the necessary offset is applied. The signals from the Synthesiser are 37.5 MHz at 3PLAK, 40.5 to 67.5 MHz at 3PLAJ, 2-3 MHz at 3PLAH. Range switch wafers 2SA21F and 2SA20F, automatically control diode switching circuits which determine the signal paths, in unit 3, appropriate to the frequency in use.

44. Ranges 5 and 6. 1 MHz from the Frequency Standard Outfit is applied via the 1 MHz Limiter, unit 25, to a harmonic generator which produces 4 MHz. This provides the offset for 4 MHz and it is applied to the 37.5 MHz input by the third mixer to produce 33.5 MHz. This is filtered and amplified and then mixed with the 2-3 MHz input in the first mixer. The resultant 35.5 to 36.5 MHz is filtered and amplified, then routed by diode switches to the fourth mixer where it is mixed with the 40.5 to 67.5 MHz input to produce the first oscillator frequency. The 40.5 to 67.5 MHz input is amplified and filtered to reject 37.5 MHz and 33.5 MHz before it is applied to the fourth mixer.

45. Ranges 1 to 4. The standard 1 MHz input is also applied to another harmonic generator which produces 3 MHz. To obtain 1 MHz offset this is added back to 35.5 to 36.5 in the second mixer which is brought into use by the range controlled diode switches. 38.5 to 39.5 MHz is now mixed with the 40.5 to 67.5 MHz output to produce the first oscillator frequency from the fourth mixer.

46. First oscillator drive. The first oscillator output from the fourth mixer is filtered and taken from unit 3 to the F.O.S.U. Wide-band Amplifier, unit 24, which has an input impedance of 150 ohms, provides a gain of 26 dB, and produces a main output at a level of 200 mV and an impedance of 75 ohms. It also produces an additional output at 20 mV to supply a second receiver for diversity reception or for use with a VLF adaptor.

47. The main output from unit 24 is taken to the first oscillator filter, in the Oscillator Filter Assembly, where it is servo tuned by main tuning capacitors 2C89, 2C76 and the inductors for the range in use, which have been automatically selected by range switch wafers 2SA16 to 2SA19.

48. The tuned output is amplified in the First Frequency Changer, unit 21, where it is gated by range controlled diode switches to drive the appropriate frequency changer.

49. 3 MHz frequency changer drive. On ranges 5 and 6 a 3 MHz drive is taken from the 3 MHz harmonic generator, via the switched 3 MHz amplifier in unit 23, to Frequency Changer (4 MHz - 1 MHz) in unit 20. On ranges 1 to 4 the 3 MHz amplifier is biased off by -30 V from range switch wafer 2SA20B.

Final Intermediate Frequency

50. In Amplifier I.F. (1 MHz), unit 20, the 1 MHz amplifier provides a flat passband response and produces the low-level 1 MHz input to the Frequency Changer (1 MHz - 100 kHz). The high-level 1.1 MHz input is provided by the 100 kHz Oscillator Board, unit 22, via the 1.1 MHz amplifier in unit 23. The frequency changer output is the final i.f. at 100 kHz to Crystal Filter Assembly, unit 13.

Fine Tuning

51. In unit 22 a standard frequency of 1 MHz from unit 25 is mixed with 100 kHz to provide the 1.1 MHz output. The 100 kHz is either from the Synthesiser or from a local crystal oscillator, depending on the position of the FINE TUNING control 1SA.

33. Operation of any Synthesiser decade control momentarily closes -30 V and -22 V switches in unit 6 and energises the tune servo. A servo off-null detector in unit 4 holds the switches closed to maintain the supplies for half a second after the servo has nulled, when the switches are opened.

34. While the range switch is moving from one position to another, wafer 2SA20B disconnects -30 V from the triggering circuits. This ensures that the -30 V and -22 V switches stay closed for half a second after the range switch stops at a position.

35. Ledex protection. A current overload switch in Panel Receiver Auxiliary Circuits, unit 6, energises and de-energises the Ledex protection relay 1RLB if the rotary solenoid 2SA is jammed. 1RLB1 is normally made and connects the supply to 2SA.

36. The overload switch, transistor 6VT9, is controlled by the voltage developed across current sensing resistor 6R27 which is in series with 2SA. So if 2SA is jammed, the current through it increases until enough voltage is produced across 6R27 to switch on 6VT9, energise 1RLB, and break 1RLB1 to switch off the Ledex supply. 6VT9 is then cut off, the current in 1RLB falls until it is de-energised, and 1RLB1 makes to restore the supply. This cycle is repeated until the fault is cleared.

37. When 1RLB1 breaks, 1RLB2 makes to switch on the CUTOUT lamp, which therefore flashes on and off while the Ledex motor is jammed.

FREQUENCY CONVERSION

Figures 1.6, 1.9

Range Dependent Intermediate Frequencies

38. For frequencies below 8 MHz, on frequency ranges 1 to 4, a double superheterodyne system is used with a first i.f. of 1 MHz. For frequencies above 8 MHz, on frequency ranges 5 and 6, a triple superheterodyne system is used with a first i.f. of 4 MHz which is again changed to produce an i.f. of 1 MHz. For all frequencies a final i.f. of 100 kHz is used.

39. The appropriate circuit is automatically selected by range switch wafer 2SA20B which controls diode switches 21MR2, 20MR7 and 21MR1, 20MR8 which act as a double-pole change-over switch.

40. Ranges 1 to 4. 21MR1 and 20MR8 are open. 21MR2 and 20MR7 are closed by -30 V via 2SA20B. The first oscillator frequency is gated by 21MR2 to the 1 MHz frequency changer 21MR3 to 21MR6, where it is mixed with the tuned r.f. input to produce an i.f. of 1 MHz, which is gated by 20MR7 to a 1 MHz tuned amplifier.

41. Ranges 5 and 6. 21MR2 and 20MR7 are open. 21MR1 and 2MR8 are closed by -30 V via 2SA20B. The first oscillator frequency is gated by 21MR1 to the 4 MHz frequency changer 21MR7 to 21MR10 where it is mixed with the tuned r.f. input to produce an i.f. of 4 MHz. This is crystal filtered and amplified before being mixed with 3 MHz in the 4 MHz - 1 MHz frequency changer 20MR2 to 20MR5. The resulting i.f. of 1 MHz is now gated by 20MR8 to the 1 MHz tuned amplifier.

Frequency Off-setting

42. The local oscillator frequency required to produce the first i.f. is the frequency set up on the Synthesiser, offset by 1 MHz or 4 MHz. The frequencies required are therefore:

(a) 0.24 + 1 MHz to 7.9999 + 1 MHz = 1.24 MHz to 8.9999 MHz on ranges 1 to 4.

(b) 8.0 + 4 MHz to 27.9999 + 4 MHz = 12.0 MHz to 31.9999 MHz on ranges 5 and 6.

Automatic Gain Control

61. The band-pass tuned amplifier output from unit 10 is processed in unit 8(8A) to produce a d.c. voltage for automatic gain control of the Amplifier I.F. Unit 9(9A) similarly provides A.G.C. for unit 11. A.G.C. for the receiver r.f. amplifiers is provided by combining the outputs of units 8(8A) and 9(9A) so that the control voltage is governed by the higher level of the two sidebands.

62. In the Panel Automatic Gain Control the A.G.C. voltage is produced by rectifying the 100 kHz i.f. input and processing the d.c. voltage for different modes of operation. This is done by charging and discharging an A.G.C. reservoir capacitor through paths with different time constants. The time constants, determined by the position of system switches on the front panel, are shown in Table 1.3.

Table 1.3 A.G.C. Tune Constants

PURPOSE	SSB MCW CW	FST DATA	DSB	SWITCH WAFER	
				UNIT 8	UNIT 9
ATTACK	FAST	FAST	SLOW	1SD1F(d)	-
HOLD	LONG	SHORT	SHORT	1SD3F	1SF1F(a)
DECAY	SLOW	FAST	SLOW	1SD2F	1SF1F(b)

63. Because there is no carrier on ssb the rectified A.G.C. voltage depends on the peaks of the received signal and a fast attack time constant is required. For dsb operation the A.G.C. voltage depends on the carrier level and a slow attack time constant is needed. Separate rectifier and time constant filter circuits are therefore used, selected in unit 8(8A) by 1SD1F(d) via switched amplifiers. On lsb the long time constant filter circuit is not used.

64. The output from the circuit in use is applied by emitter followers to a reservoir charging circuit which provides the primary time constant, for long hold and decay times. Surges in the input signal are provided for in a by-pass circuit which reduces the gain of the receiver until the reservoir capacitor is charged.

65. Trigger circuits operate at threshold level, which is about 3 dB below the onset of A.G.C., to initiate and control the discharge of the reservoir capacitor.

66. 1SD3F or 1SF1F(a) determines the hold time ie the time between the signal falling below the threshold level and the reservoir capacitor starting to discharge. On dsb, fst and data one capacitor in parallel with the reservoir capacitor produces a short hold time and a shunting resistor ensures that the A.G.C. voltage falls at a controlled rate when the signal level falls. On ssb, mcw and cw two more capacitors in parallel with the reservoir capacitor produce a long hold tune.

67. 1SD2F or 1SF1F(b) determines the discharge rate of the reservoir capacitor by changing the resistance of its discharge path. On fst and data a 120 ohm resistor produces a fast decay, and on ssb, dsb, mcw and cw a 100 kohm resistor produces a slow decay.

52. 1SA2F applies -30 V to one of two diode switches so that the 100 kHz is from the Synthesiser via 2 PLAE when 1SA is at 0, and from the oscillator when 1SA is at any other position. When the oscillator is in use, the nominal 1.1 MHz can be "pulled" in 10 Hz steps by 1SA1F which varies the 0 V to 70 V supply to a varactor frequency control.

Standard 1 MHz Input

53. Because the level of the 1 MHz input from the Frequency Standard Outfit at 2PLAG may vary, it is limited by the 1 MHz Limiter, unit 25, which will reduce a variation of 10 dB in input level to one of 3 dB in output level.

54. In unit 25 two separate circuits, each comprising a buffer amplifier, a diode limiter and an output transformer, are used to produce two isolated 1 MHz (Limited) outputs. One output is for the 100 kHz Oscillator, unit 22, and the other for Frequency Offset Unit, unit 3. A third output, from the same source as that for unit 3, provides a test signal and a d.c. switching potential to the First Frequency Changer, unit 21.

I.F. AMPLIFICATION AND DEMODULATION

Figures 1.7, 1.10

Sideband Filter Selection

55. The main selectivity of the Receiver is by crystal sideband filters at 100 kHz. The usb, dsb channel has four filters with bandwidths appropriate to fst, cw, dsb, usb. The lsb channel has one filter.

56. The five sideband filters are in Crystal Filter Assembly, unit 13, to which 100 kHz i.f. from Amplifier I.F., unit 20, is applied at 13PLEQ. The filters are selected via Panel Filter Switching, unit 12, which plugs into unit 13.

57. In unit 13 the 100 kHz input at 12PLL6 is fed to two amplfiers, one for the usb, dsb channel and one for the lsb channel. The amplified outputs are gated through the sideband filters by pairs of diode switches to which a switching potential of -30 V is applied by system switch wafers 1SD1F and 1SF1F, via routing diodes in Diode Board DB1, unit 18. The switching arrangements ensure that lsb is not available when DSB or MCW is selected on 1SD. In both channels the filtered i.f. is amplified to produce the usb, dsb output at 13PLEL and the lsb output at 13PLEM. Each output is subsequently processed through separate but similar channels.

Sideband I.F. Amplification

58. The 100 kHz upper sideband, double sideband i.f. from unit 13 is amplified, by up to 70 dB, in Amplifier Intermediate Frequency unit 10 which is subjected to A.G.C. by Panel Automatic Gain Control unit 8(8A). The amplifier has an A.G.C. range of 80 dB which includes a forward A.G.C. circuit which reduces the error output over the whole A.G.C. range to zero.

59. The 100 kHz lower sideband i.f. from unit 13 is similarly amplified by units 11 and 9(9A) which are the same as units 10 and 8(8A), but the usb facilities are not used.

60. In unit 10 A.G.C. is applied to the first three stages of a four stage band-pass tuned amplifier. The fourth stage is a voltage feedback amplifier which provides a low impedance output to operate the forward A.G.C. circuit and to supply unit 8(8A). The output stage of the i.f. amplifier provides an output of low impedance for ssb operation and one of high impedance for dsb operation. A squelch circuit controlled by unit 8(8A) can be switched IN or OUT by the SQUELCH switch on the front panel.

80. A.F. from the 1sb demodulator is amplified and filtered through a 10 kHz low-pass filter. The filtered a.f. is amplified, then in Panel Demodulator Unit 7 (5820-99-519-7029), is limited to remove noisy spikes. The limiting level is set just clear of the normal operational level and operates only on short bursts of signal when A.G.C. is ineffective. An emitter follower provides a.f. outputs for line amplification and for local monitoring.

NOTE. In Panel Demodulator Unit 7A (5820-99-758-9179) the limiter stage is omitted. The filtered a.f. is amplified then fed to the emitter-follower.

81. A.F. from the usb demodulator or the dsb detector is treated in the same way, through an identical circuit which is switched to one or the other by diode switches. The switches act as a single pole change-over switch and they are operated by -30 V switching potential from system switch wafer SD1F(d) via Diode Board DB1.

AUDIO FREQUENCY OUTPUT

A.F. Amplification

Figures 1.8, 1.10

82. The usb, dsb and 1sb audio frequency outputs from Panel Demodulator, unit 7(7A), are amplified in Amplifier Audio Frequency, unit 5(5A), to drive a loudspeaker on the front panel and headsets at local or remote positions. Signal paths in unit 7(7A) are determined by diode switches operated by -30 V via front panel switches.

83. Change-over switch 1SM applies -30 V to one of two diode switches in unit 5(5A), so that the selected input is routed via volume control 1RV2A to the loudspeaker amplifier which can produce an output of 1 W for a 30% modulated dsb signal.

84. Separate and identical a.f. amplifiers provide balanced line outputs to one local and two remote positions. Each amplifier has fixed gain and an output impedance of 200 ohms which allows the sidetone output of an associated Modulator Tuning Unit to be connected in parallel. The usb, dsb or 1sb input is routed to one of the line amplifiers by diode switching.

85. For reception on USB/DSB, -30 V from 1SD1F(b) is switched by 1SC1F(b) on LOC, REM1 or REM2 to close the diode switch which gates the usb, dsb input to the selected amplifier.

86. For reception on LSB when 1SD is at OFF, SSB, CW, FST or DATA, -30 V from 1SD1F is connected via Diode Board DB1 to 1SF1F then switched by 1SE1F(b) on LOC, REM1 or REM2 to close the diode switch which gates the 1sb input to the selected amplifier.

87. If both channel inputs are switched to the same amplifier, the two input circuits load each other to prevent overloading and distortion in the amplifier.

A.F. Monitoring

88. A.F. outputs from Panel Demodulator, unit 7(7A), can be monitored at headset jacks, 1JKA on RECEIVE USB/DSB and 1JKB on receive LSB.

89. The a.f. output from any line amplifier in Amplifier Audio Frequency, unit 5(5A), can be monitored at the H/SETS jack 1JKC and socket 1SKTAX on the MONITORING front panel.

90. The headset switch 1SJ is switched to USB/DSB or LSB and applies -30 V to 1SC1F(a) or 1SE1F(a). Depending on the position of 1SC or 1SE, -30 V then closes the diode switch which gates the selected output via 1RV2B to an emitter follower circuit in Panel Receive Auxiliary Circuits, unit 6. This provides a low impedance drive at 1JKC and 1SKTAX. 1RV2B is the headset volume control, ganged to the loudspeaker volume control 1RV2A. Both are operated by the VOLUME control.

68. When the signal reaches threshold level the first trigger operates and the hold time capacitors are charged. When the signal level falls below threshold level the hold time capacitors discharge, the second trigger operates and allows the reservoir capacitor to discharge through the discharge circuit at the selected rate.

69. The second trigger also provides the squelch control, at a threshold level 3 dB below the A.G.C. threshold, for the associated Amplifier I.F.

70. The A.G.C. drive is distributed via a network of isolating diodes.

71. A large range of gain control is provided independently on each channel so that satisfactory performance can be obtained on isb with the two sideband signals differing in level by 40 dB. For received signal levels between 1 µV and 1 V the receiver A.G.C. holds the usb or lsb channel output to the same peak envelope power.

R.F. Gain Control and Receiver Muting

72. Gain control and muting is achieved by applying a negative voltage to the base of emitter follower VT6 in the appropriate Panel Automatic Gain Control, and thus to the A.G.C. line. Suitable voltages are available from the local R.F. GAIN control, remote r.f. gain controls, the MUTE switch and the Overload Protection Unit. These voltages are applied to routing diodes on Diode Board DB2, unit 17, and all of them may be present at the same time. The diode connected to the most negative voltage will be forward biased and that line will take control, because the other diodes will be reverse biased.

73. The r.f. gain control voltage, -10 V maximum, is from the front panel R.F. GAIN control 1RV1 or from remote gain controls REM1, REM2. The components associated with 1RV1 are on unit 17. For usb and dsb operation (with unit 8(8A)) REM1, REM2 are switched in by 1SD2B and one of them is selected by 1SC1B. For lsb operation (with unit 9(9A)) REM1, REM2 are switched in by 1SD3B and 1SF1B, and one of them is selected by 1SE1B.

74. Each remote gain control varies the gain of its own channel without varying the gain of the other channel or materially affecting the r.f. gain of the receiver. The front panel R.F. GAIN control, however, affects both channels equally so if it produces a more negative voltage than either of the remote controls it will override them.

75. For simplex operation the MUTE switch 1SH is normally ON so that -30 V is applied to mute the receiver during transmission from a local transmitter.

76. If the overload prevention relay 2RLA is de-energised, 2RLA2 breaks and -30 V is applied, from unit 17, to mute the receiver.

Demodulation

77. The sideband outputs from Amplifiers I.F., units 10 and 11, are demodulated in Panel Demodulator, unit 7.

78. The low impedance, usb and lsb outputs are demodulated in separate but similar balanced modulators for which 100 kHz from the Frequency Synthesiser is amplified to provide the re-insertion oscillation. In Outfit CJM this 100 kHz is taken directly from the Synthesiser but in Type 641 it is taken via the 100 kHz switch.

79. The high impedance double sideband output is amplified and then demodulated by a conventional diode detector. When reception is on dsb, the 100 kHz re-insertion carrier for ssb is disconnected by a diode switch which is reverse biased by -30 V from SD1F(d) via Diode Board DB1 unit 18.

1 MHz Metering Board

96. This is a small printed wiring board mounted on the base of the parent cabinet. It carries a rectifier circuit which provides a smoothed d.c. output proportional to the level of the 1 MHz standard input. It is this d.c. level which is checked on position 1 of the METERING switch.

POWER DISTRIBUTION

Figure 1.13

A.C. Mains Supply

97. The receiver can be used with 50 to 60 Hz supply voltages from 200 V to 260 V or 100 V to 130 V, depending on the connections of the mains transformer 14TR1. Normally, power consumption is about 70 W but during tuning it may reach 150 W.

Converted Supplies

98. The power supplies shown in Table 1.5 are obtained from the internal Power Supply, unit 14, which includes Stabiliser Boards, units 15 and 16.

Table 1.5 Power Supplies

SUPPLY	DESTINATION
+200 V H.T.) EARTH)	2V1, 2V2
+70 V	FINE TUNING control via 1RV4
+41 V -41 V	Rotary solenoid 2SA via 1RLB1 Unit 6. Ultimately 2SA
+30 V	Units 2, 3, 5, 7 to 11, 13 Audio transformer 1T1 METERING switch 1SB External circuits
-30 V	Units 2, 4 to 11, 17 External circuits
6.3 V a.c.	2V1, 2V2 heaters 1LP3 via 1RLB2 1LP8 via 1SD 1LP9 via 1SD, 1SF

99. All d.c. supplies are stabilised except +41 V, -41 V.

100. If the load on the +30 V or -30 V stabilised supply exceeds 1.5 A an overload protection circuit operates and clamps the output to zero.

101. A -22 V during tune supply to Panel Servo Supply, unit 4, is derived from the -41 V unstabilised supply via Panel Receiver Auxiliary Circuits, unit 6.

91. If both line selector switches 1SC and 1SE are set to the same position the selected line amplifier output can be monitored with 1SJ switched to either USB/DSB or LSB, despite the fact that the signal may be available on only one channel.

92. Connection of a sidetone output from an associated Modulator Tuning Unit to the local a.f. line allows both transmission and reception to be monitored.

METERING TESTS

Figures 1.6, 1.7, 1.11

93. Major parameters can be checked on the front panel micro-ammeter 1M1 which is connected to appropriate circuits by the 20-way METERING switch 1SB. For some tests the meter is switched in series with resistors and used as a voltmeter, for others it is switched to diode detectors and used as an r.f. voltmeter. The test circuits are arranged, however, so that nominal meter readings indicate correct values.

94. The purpose of each switch position is described briefly in Table 1.4. Full details are given in Part 5C.

Table 1.4 METERING Switch Positions

POSN.	TALLY	METER INDICATION TO PROVE:-
1	1 MHz	1 MHz standard at cabinet Metering Board
2	RANGE	Rotary solenoid drive to range switches
3	+230 V	
4	+30 V — SUPPLIES	Supplies in Power Supply
5	-30 V	
6	1K1 + 2	R.F. cathode current on full gain
7	37.5 MHz	
8	VAR OSC — FROM SYN	Frequency Synthesiser inputs to F.O.S.U.
9	2-3 MHz	
10	1st OSC	First Oscillator Output
11	3 MHz — FREQ. CH. DRIVES	3 MHz drive to Frequency Changer (4 MHz - 1 MHz)
12	1.1 MHz	1.1 MHz drive to Frequency Changer (1 MHz - 100 kHz)
13	100 kHz	100 kHz drive to Panel Demodulator
14	USB — A.G.C. DET.	A.G.C. rectifier output on Panel A.G.C. (USB)
15	LSB	A.G.C. rectifier output on Panel A.G.C. (LSB)
16	USB — A.G.C.	A.G.C. or R.F. GAIN output from Panel A.G.C. (USB)
17	LSB	A.G.C. or R.F. GAIN output from Panel A.G.C. (LSB)
18	4 MHz	
19	1 MHz — IF TEST ON DSB	Operation of receiver. Carrier frequency injected then monitored at A.G.C. rectifier.
20	100 kHz	

95. A special procedure, detailed in Part 5C, must be followed to carry out a test on switch position 18, 19 or 20. For the test, the receiver is switched to dsb operation and 4 MHz, 1 MHz or 100 kHz is gated to the appropriate circuit by a diode switch, operated by -30 V via 1SB on the selected position. The carrier thus injected is checked, via 1SB, at the A.G.C. rectifier output on Panel Automatic Gain Control (usb), unit 8(8A).

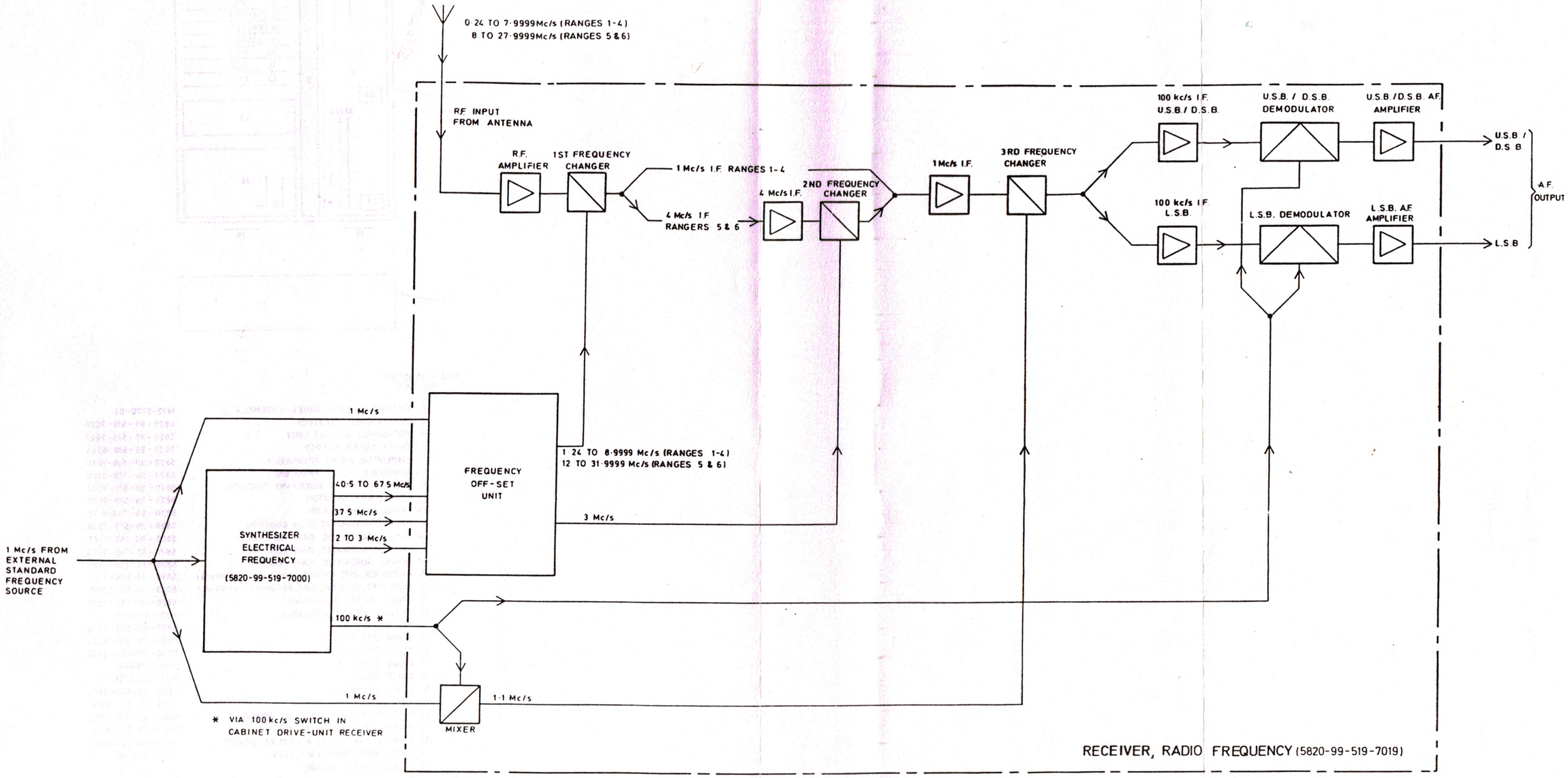
NOTE Receiver performance will be adversely affected if the METERING switch is left at a position marked in red ie 10, 11, 12, 13, 18, 19 or 20.

DIODE BOARDS

Figures 1.4, 1.5

102. Diode Board DB1, unit 18, carries diodes which are switched in conjunction with 1SD and 1SF to route -30 V switching potential to the selected circuit.

103. Diode Board DB2, unit 17, carries routing diodes connected so that the most negative of a number of control voltages takes precedence.

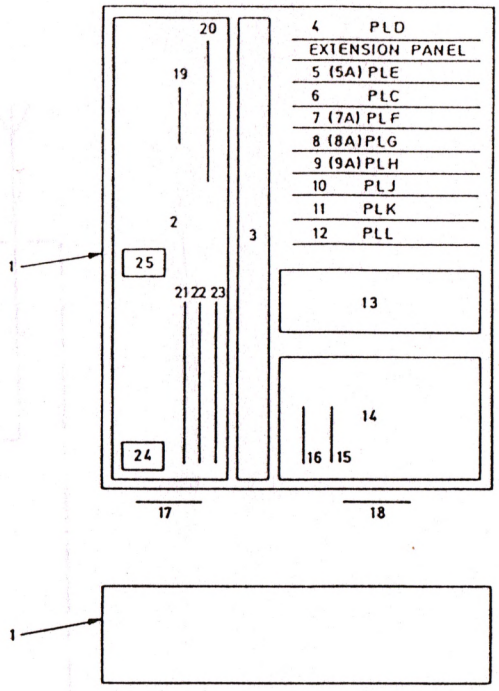


RECEIVING EQUIPMENT (FREQUENCY CHANGING & DEMODULATION)
SIMPLIFIED BLOCK DIAGRAM

FIG. 1.1



FIG 1.2

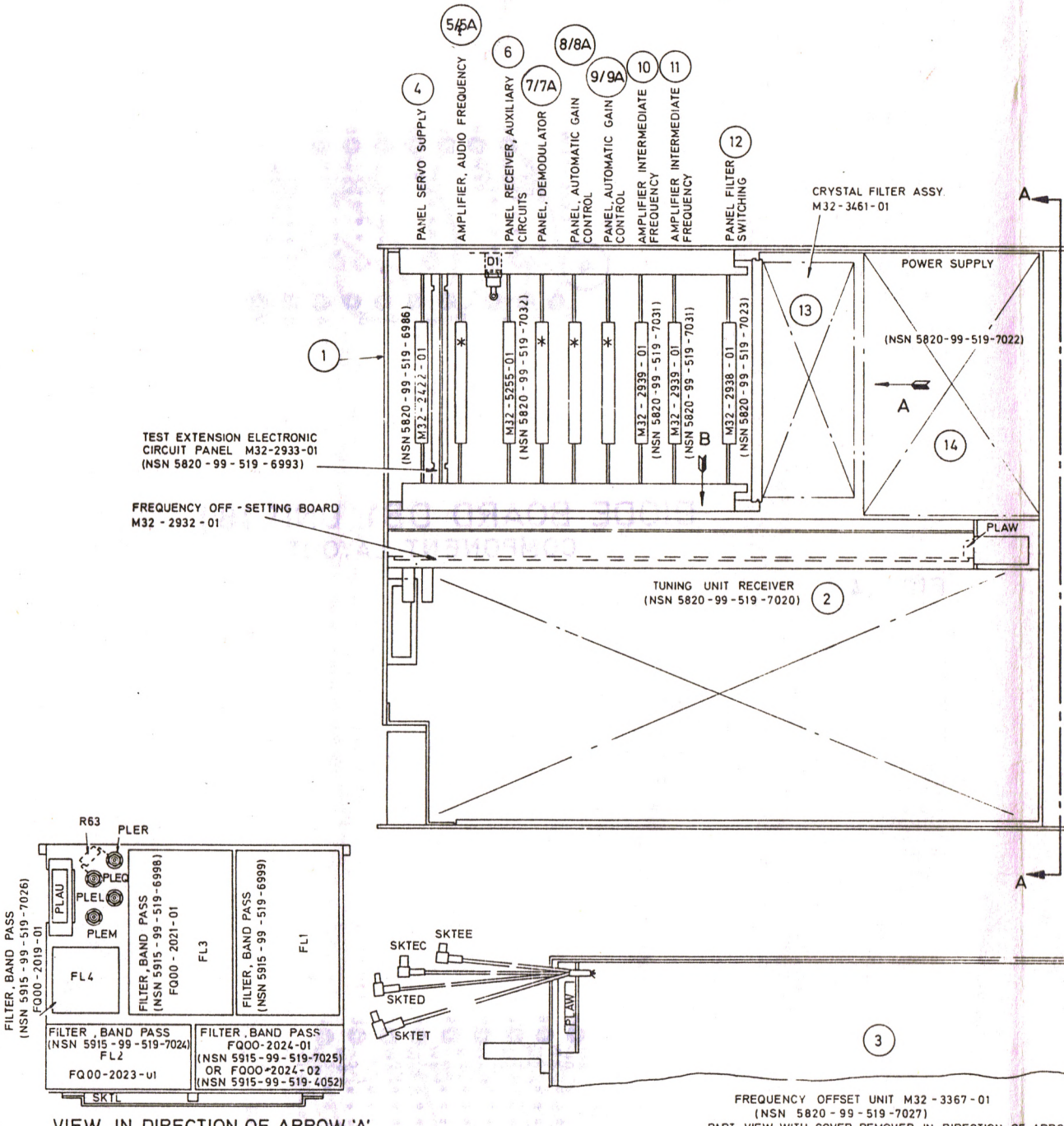


SUB – ASSEMBLY
OR UNIT :-

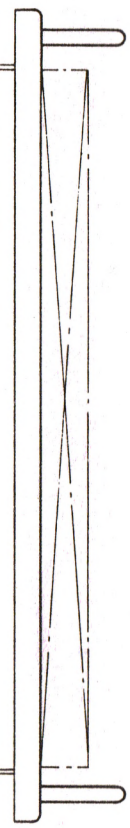
1	CHASSIS & FRONT PANEL ASSEMBLY	M32-5170-01
2	TUNING UNIT, RECEIVER	5820-99-519-7020
3	FREQUENCY OFFSET UNIT	5820-99-519-7027
4	PANEL, SERVO SUPPLY	5820-99-519-6986
5	AMPLIFIER, AUDIO FREQUENCY	5820-99-519-7030
5A	AMPLIFIER, AUDIO FREQUENCY	5820-99-758-9180
6	PANEL, RECEIVER AUXILIARY CIRCUITS	5820-99-519-7032
7	PANEL, DEMODULATOR	5820-99-519-7029
7A	PANEL, DEMODULATOR	5820-99-758-9179
8	PANEL, AUTOMATIC GAIN CONTROL	5820-99-519-7028
8A	PANEL, AUTOMATIC GAIN CONTROL	5820-99-758-9181
9	PANEL, AUTOMATIC GAIN CONTROL	5820-99-519-7028
9A	PANEL, AUTOMATIC GAIN CONTROL	5820-99-758-9181
10	AMPLIFIER, INTERMEDIATE FREQUENCY (100kc/s)	5820-99-519-7031
11	AMPLIFIER, INTERMEDIATE FREQUENCY (100kc/s)	5820-99-519-7031
12	PANEL, FILTER SWITCHING	5820-99-519-7023
13	CRYSTAL FILTER ASSEMBLY	M32-3461-01
14	POWER SUPPLY	5820-99-519-7022
15	STABILIZER BOARD	5820-99-521-9421
16	STABILIZER BOARD	5820-99-521-9422
17	DIODE BOARD 2	M32-5254-01
18	DIODE BOARD 1	M32-5253-01
19	4 Mc/s I.F. BOARD	5820-99-521-9418
20	1 Mc/s I.F. BOARD	5820-99-521-9416
21	FIRST FREQUENCY CHANGER BOARD	5998-99-016-0633
22	100 kc/s OSCILLATOR BOARD	5820-99-521-9420
23	1·1 Mc/s AND 3 Mc/s AMPLIFIER BOARD	5820-99-521-9419
24	F.O.S.U. WIDEBAND AMPLIFIER	M32-5269-01
25	1 Mc/s LIMITER BOARD	M32-3766-01

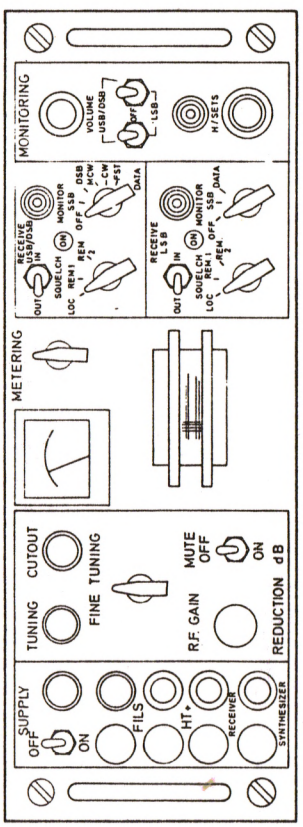
MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

RECEIVER R.F. 5820-99-519-7019
COMPONENT LOCATION

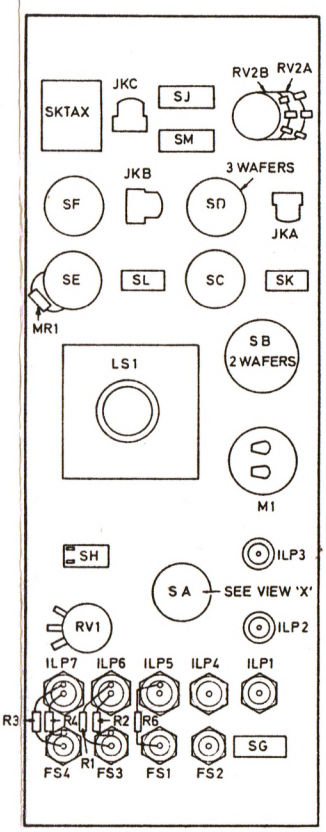

4
PANEL SERVO SUPPLY
5/5A
AMPLIFIER, AUDIO FREQUENCY
6
PANEL RECEIVER, AUXILIARY CIRCUITS
7/7A
PANEL, DEMODULATOR
8/8A
PANEL, AUTOMATIC GAIN CONTROL
9/9A
PANEL, AUTOMATIC GAIN CONTROL
10
AMPLIFIER INTERMEDIATE FREQUENCY
11
AMPLIFIER INTERMEDIATE FREQUENCY
12
PANEL FILTER SWITCHING
CRYSTAL FILTER ASSY M32-3461-01
POWER SUPPLY
(NSN 5820-99-519-7022)
13
14
1
(NSN 5820-99-519-6986)
M32-2422-01
M32-5255-01
(NSN 5820-99-519-7032)
M32-2939-01
(NSN 5820-99-519-7031)
M32-2939-01
(NSN 5820-99-519-7031)
M32-2938-01
(NSN 5820-99-519-7023)
TEST EXTENSION ELECTRONIC CIRCUIT PANEL M32-2933-01 (NSN 5820-99-519-6993)
FREQUENCY OFF-SETTING BOARD M32-2932-01
PLAW
TUNING UNIT RECEIVER (NSN 5820-99-519-7020)
2
A
B
R63
PLER
PLEQ
PLEL
PLEM
PLAU
FILTER, BAND PASS (NSN 5915-99-519-7026) FQ00-2019-01
FL4
FILTER, BAND PASS (NSN 5915-99-519-6998) FQ00-2021-01
FL3
FILTER, BAND PASS (NSN 5915-99-519-6999)
FL1
FILTER, BAND PASS (NSN 5915-99-519-7024) FL2 FQ00-2023-01
FILTER, BAND PASS FQ00-2024-01 (NSN 5915-99-519-7025) OR FQ00-2024-02 (NSN 5915-99-519-4052)
SKTL
SKTEC
SKTEE
SKTED
SKTET
PLAW
3
FREQUENCY OFFSET UNIT M32-3367-01 (NSN 5820-99-519-7027)
PART VIEW WITH COVER REMOVED, IN DIRECTION OF ARRO
VIEW IN DIRECTION OF ARROW 'A'

* UNIT No	NSN	BOARD IDENTITY
5	5820-99-519-7030	M32 - 2942 - 01
5A	5820-99-758-9180	M33 - 9647 - 01
7	5820-99-519-7029	M32 - 2941 - 01
7A	5820-99-758-9179	M33 - 9648 - 01
8	5820-99-519-7028	M32 - 2940 - 01
8A	5820-99-758-9181	M33 - 9649 - 01
9	5820-99-519-7028	M32 - 2940 - 01
9A	5820-99-758-9181	M33 - 9649 - 01

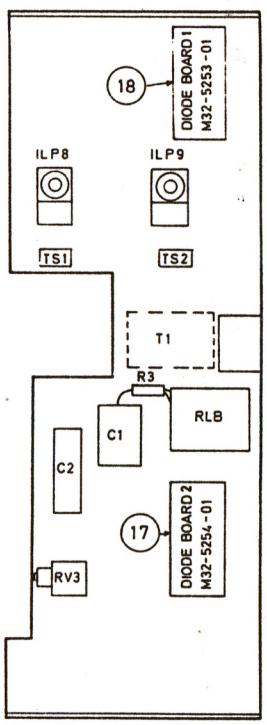




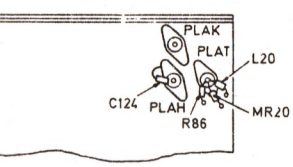
FRONT VIEW



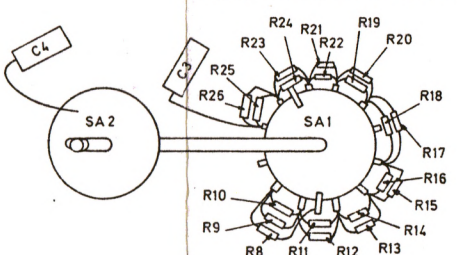
REAR VIEW OF FRONT PANEL



SECTION AT 'A - A'



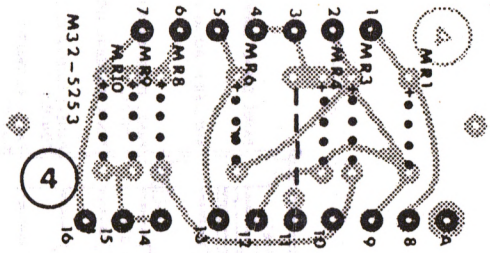
W 'B'



VIEW 'X' SHOWING COMPONENTS ASSOCIATED WITH SA1

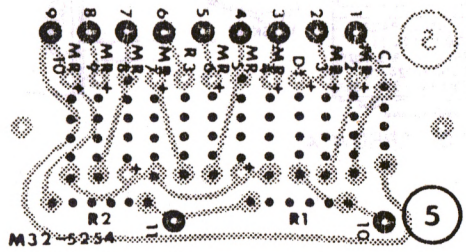
RECEIVER RADIO FREQUENCY 5820-99-519-7019
SUB – ASSEMBLY 1 COMPONENT LAYOUT

FIG. 1.3



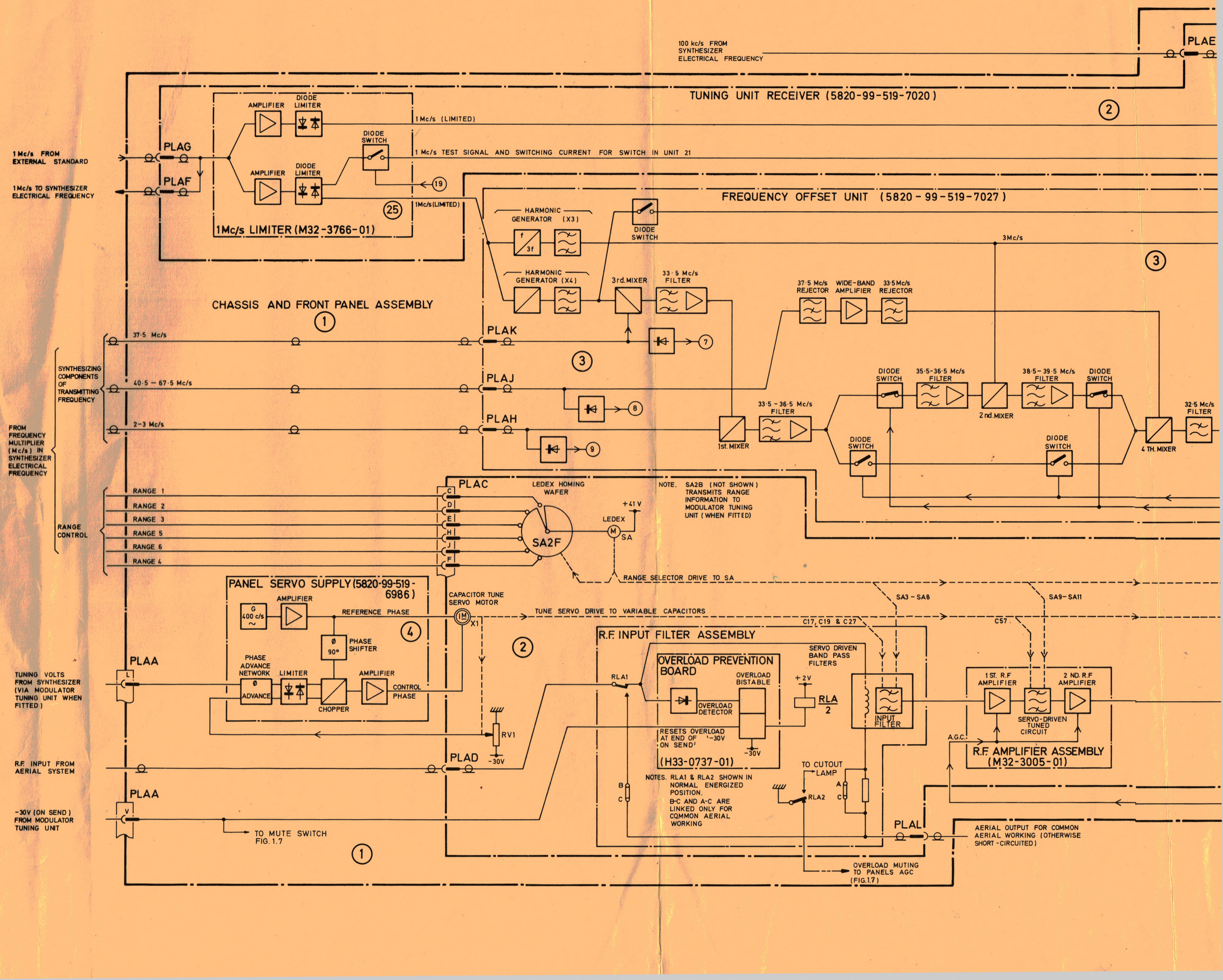
DIODE BOARD DB1 (UNIT 18)
COMPONENT LAYOUT

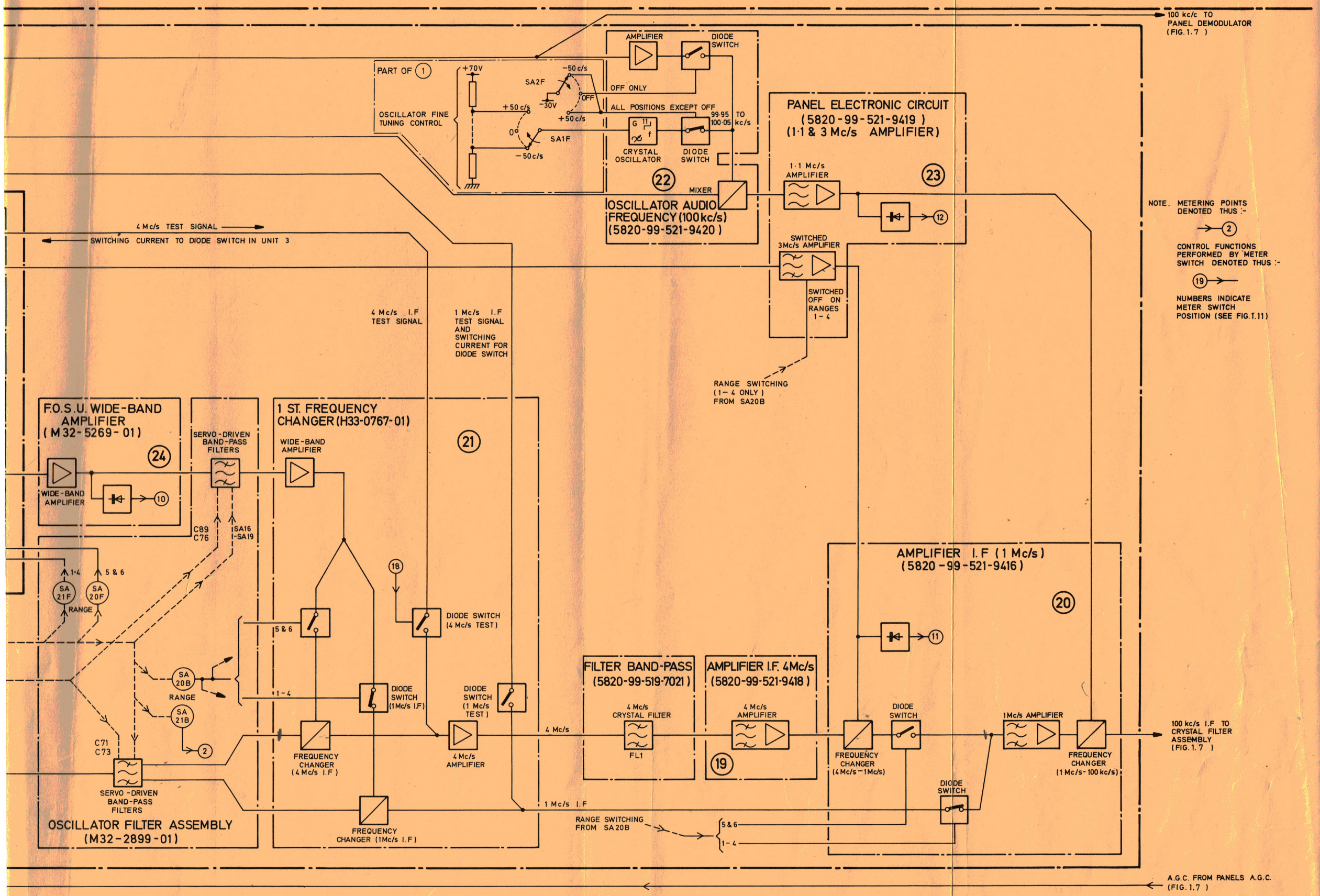
FIG 1.4



DIODE BOARD DB2 (UNIT 17)
COMPONENT LAYOUT

FIG 1.5


100 kc/s FROM SYNTHESIZER ELECTRICAL FREQUENCY
PLAE
TUNING UNIT RECEIVER (5820-99-519-7020)
2
1 Mc/s FROM EXTERNAL STANDARD
1 Mc/s TO SYNTHESIZER ELECTRICAL FREQUENCY
PLAG
PLAF
AMPLIFIER
DIODE LIMITER
AMPLIFIER
DIODE LIMITER
DIODE SWITCH
1 Mc/s (LIMITED)
1 Mc/s TEST SIGNAL AND SWITCHING CURRENT FOR SWITCH IN UNIT 21
19
25
1Mc/s(LIMITED)
1Mc/s LIMITER (M32-3766-01)
FREQUENCY OFFSET UNIT (5820-99-519-7027)
HARMONIC GENERATOR (X3)
DIODE SWITCH
3Mc/s
3
HARMONIC GENERATOR (X4)
3rd. MIXER
33·5 Mc/s FILTER
37·5 Mc/s REJECTOR
WIDE-BAND AMPLIFIER
33·5 Mc/s REJECTOR
CHASSIS AND FRONT PANEL ASSEMBLY
1
PLAK
7
3
PLAJ
8
PLAH
9
37·5 Mc/s
40·5 – 67·5 Mc/s
2–3 Mc/s
SYNTHESIZING COMPONENTS OF TRANSMITTING FREQUENCY
FROM FREQUENCY MULTIPLIER (Mc/s) IN SYNTHESIZER ELECTRICAL FREQUENCY
RANGE 1
RANGE 2
RANGE 3
RANGE 5
RANGE 6
RANGE 4
RANGE CONTROL
PLAC
C
D
E
H
J
F
LEDEX HOMING WAFER
SA2F
+41 V
LEDEX
M
SA
NOTE. SA2B (NOT SHOWN) TRANSMITS RANGE INFORMATION TO MODULATOR TUNING UNIT (WHEN FITTED)
1st. MIXER
33·5 – 36·5 Mc/s FILTER
DIODE SWITCH
35·5–36·5 Mc/s FILTER
2 nd. MIXER
38·5 – 39·5 Mc/s FILTER
DIODE SWITCH
4 TH. MIXER
32·5 Mc/s FILTER
DIODE SWITCH
DIODE SWITCH
PANEL SERVO SUPPLY (5820-99-519-6986)
G 400 c/s
AMPLIFIER
REFERENCE PHASE
4
Ø 90°
PHASE SHIFTER
PHASE ADVANCE NETWORK
Ø ADVANCE
LIMITER
CHOPPER
AMPLIFIER
CONTROL PHASE
CAPACITOR TUNE SERVO MOTOR
IM
X1
TUNE SERVO DRIVE TO VARIABLE CAPACITORS
2
RANGE SELECTOR DRIVE TO SA
SA3 – SA8
SA9 – SA11
C17, C19 & C27
C57
R.F INPUT FILTER ASSEMBLY
SERVO DRIVEN BAND PASS FILTERS
OVERLOAD PREVENTION BOARD
OVERLOAD BISTABLE
OVERLOAD DETECTOR
RESETS OVERLOAD AT END OF '-30V ON SEND'
(H33-0737-01)
+2V
RLA 2
INPUT FILTER
1ST. R.F AMPLIFIER
2 ND. R.F AMPLIFIER
SERVO-DRIVEN TUNED CIRCUIT
A.G.C.
R.F AMPLIFIER ASSEMBLY (M32-3005-01)
PLAA
L
TUNING VOLTS FROM SYNTHESIZER (VIA MODULATOR TUNING UNIT WHEN FITTED)
RV1
-30V
PLAD
R.F INPUT FROM AERIAL SYSTEM
PLAA
V
-30V (ON SEND) FROM MODULATOR TUNING UNIT
TO MUTE SWITCH FIG. 1.7
1
RLA1
RLA2
B
C
A
C
TO CUTOUT LAMP
NOTES. RLA1 & RLA2 SHOWN IN NORMAL ENERGIZED POSITION.
B-C AND A-C ARE LINKED ONLY FOR COMMON AERIAL WORKING
PLAL
AERIAL OUTPUT FOR COMMON AERIAL WORKING (OTHERWISE SHORT-CIRCUITED)
OVERLOAD MUTING TO PANELS AGC (FIG. 1.7)



MOD RECORD						
1	2	3	4	5	6	
7	8	9	10	11	12	

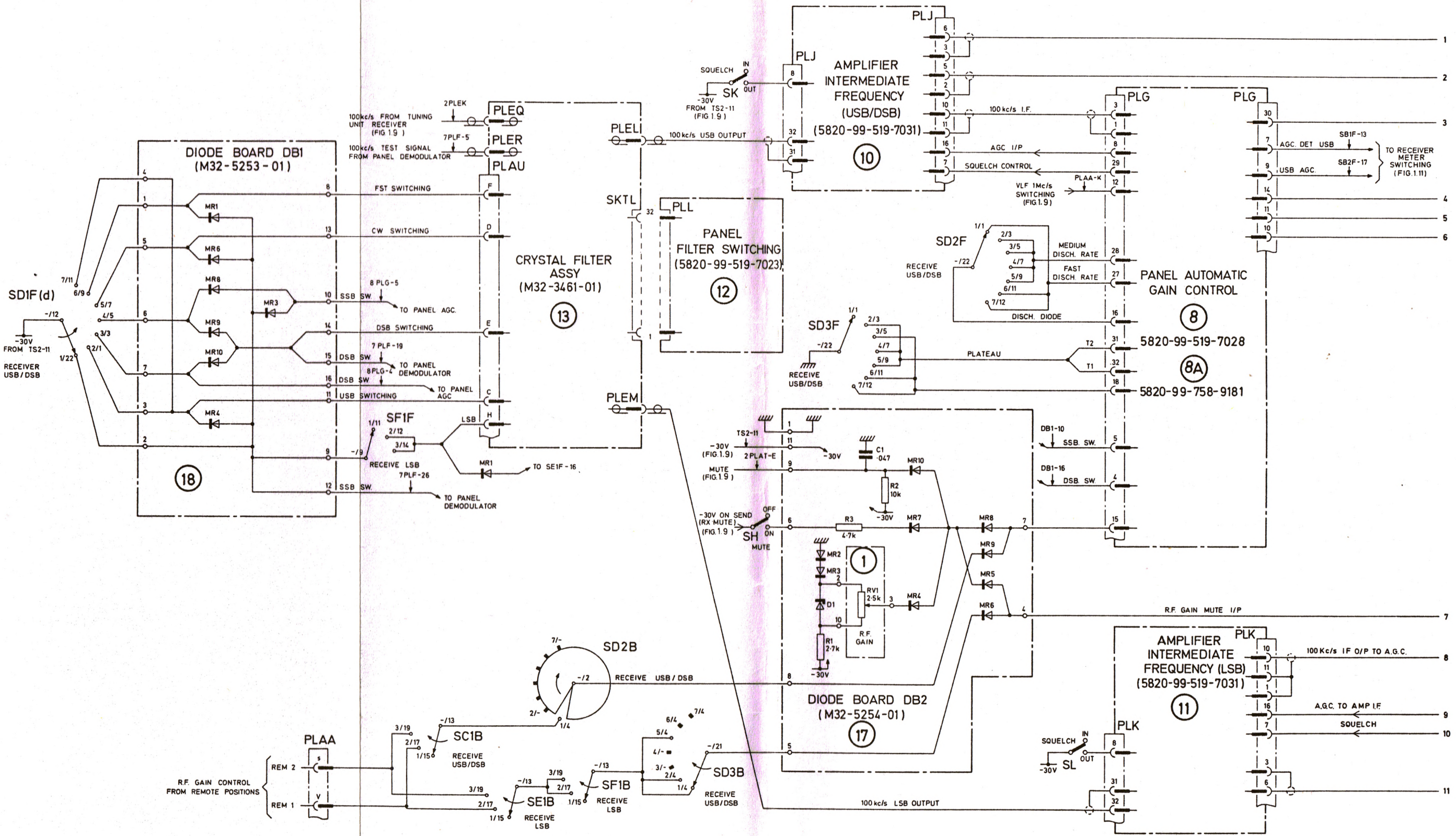
RECEIVER RADIO FREQUENCY 5820-99-519-7019

R.F & FREQ. CHANGERS BLOCK DIAGRAM

FIG. 1.6

B.R. 4147 (5) A
Amdt. 7,12,84

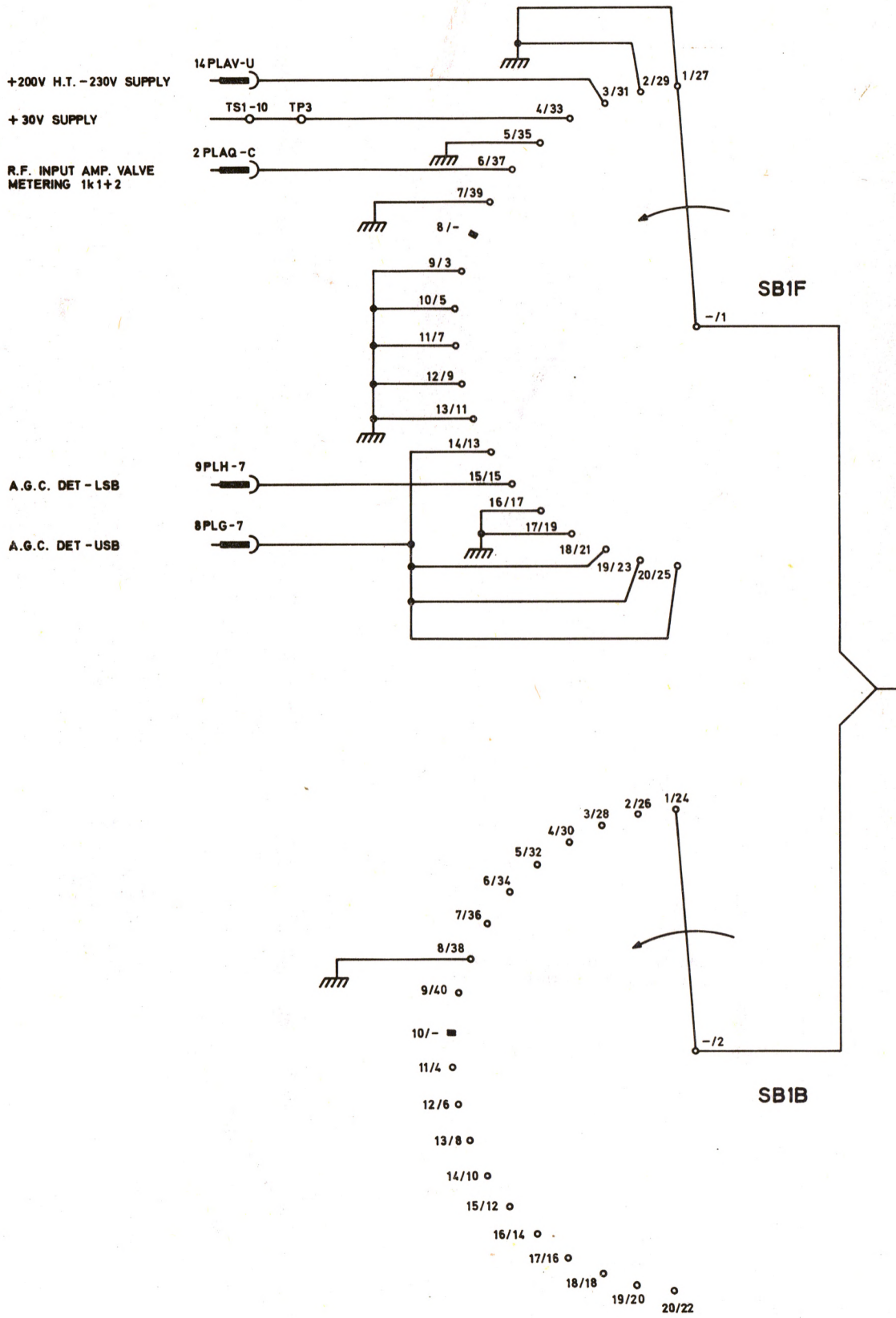
RES.	1 3 RV1 2
CAP	1
MISC.	SD1F(d) MR1 MR6 MR8 MR9 MR10 MR4 MR3 SF1F SC1B MR1 SE1B SD2B SF1B SD3B SH MR2 MR3 D1 SD3F MR10 MR7 MR4 SD2F MR8 MR9 MR5 MR6

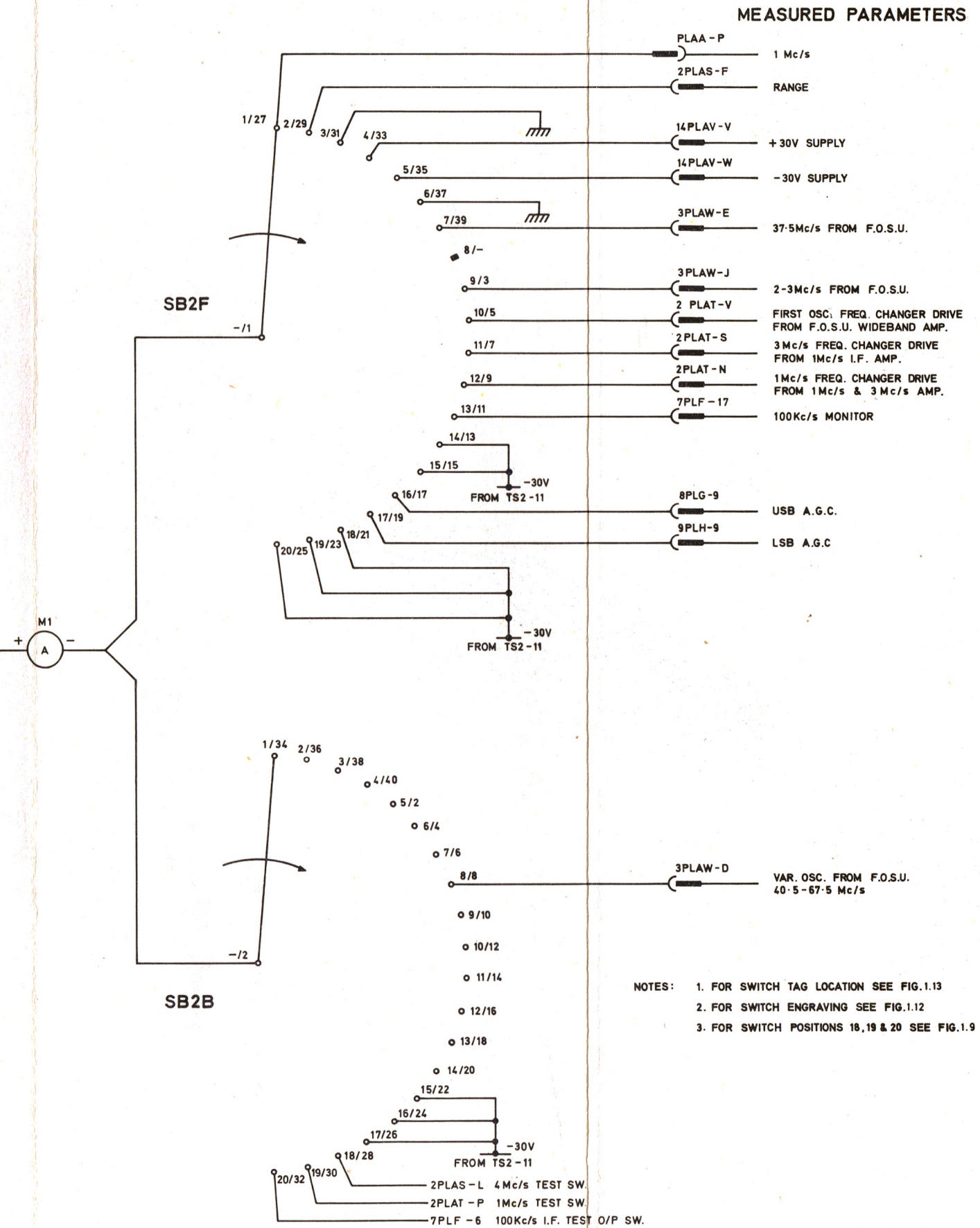


RECEIVER RADIO FREQUENCY 5820-99-519-7019
SUB-ASSEMBLY 1 (SIGNAL FLOW - PART 2) CIRCUIT DIAGRAM

FIG. 1.10A

MEASURED PARAMETERS





NOTES:
1. FOR SWITCH TAG LOCATION SEE FIG.1.13
2. FOR SWITCH ENGRAVING SEE FIG.1.12
3. FOR SWITCH POSITIONS 18,19 & 20 SEE FIG.1.9

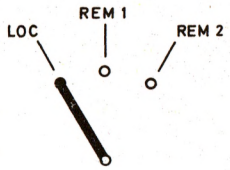
MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

RECEIVER, RADIO FREQUENCY 5820-99-519-7019

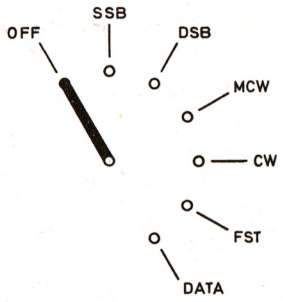
SUB-ASSEMBLY 1 (METER SWITCHING) CIRCUIT DIAGRAM

FIG.1.11

RECEIVE USB/DSB

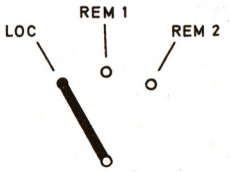


SC

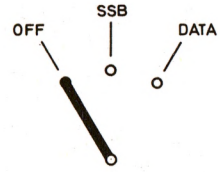


SD

RECEIVE LSB

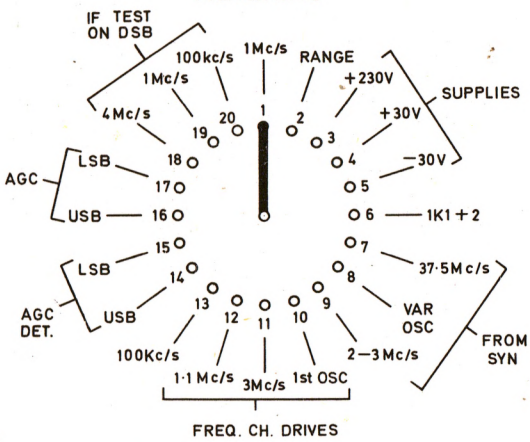


SE



SF

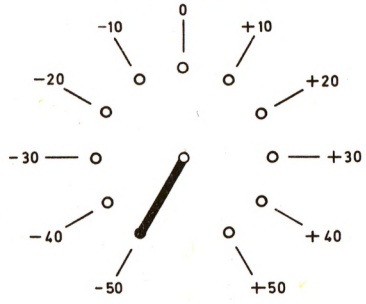
METERING



SB

NOTE:
SWITCHES ARE SHOWN IN POSITIONS AS DRAWN ON CIRCUIT DIAGRAM.

FINE TUNING



SA

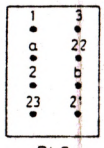
RECEIVER RADIO FREQUENCY M30-1052-01

SWITCH DIAGRAM

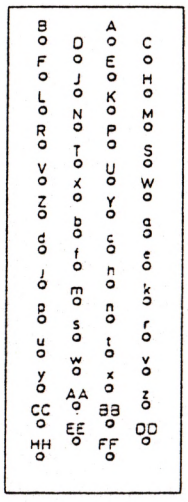
FIG.1.12

BR 4147 (5) A
Amdt 7, 12, 84

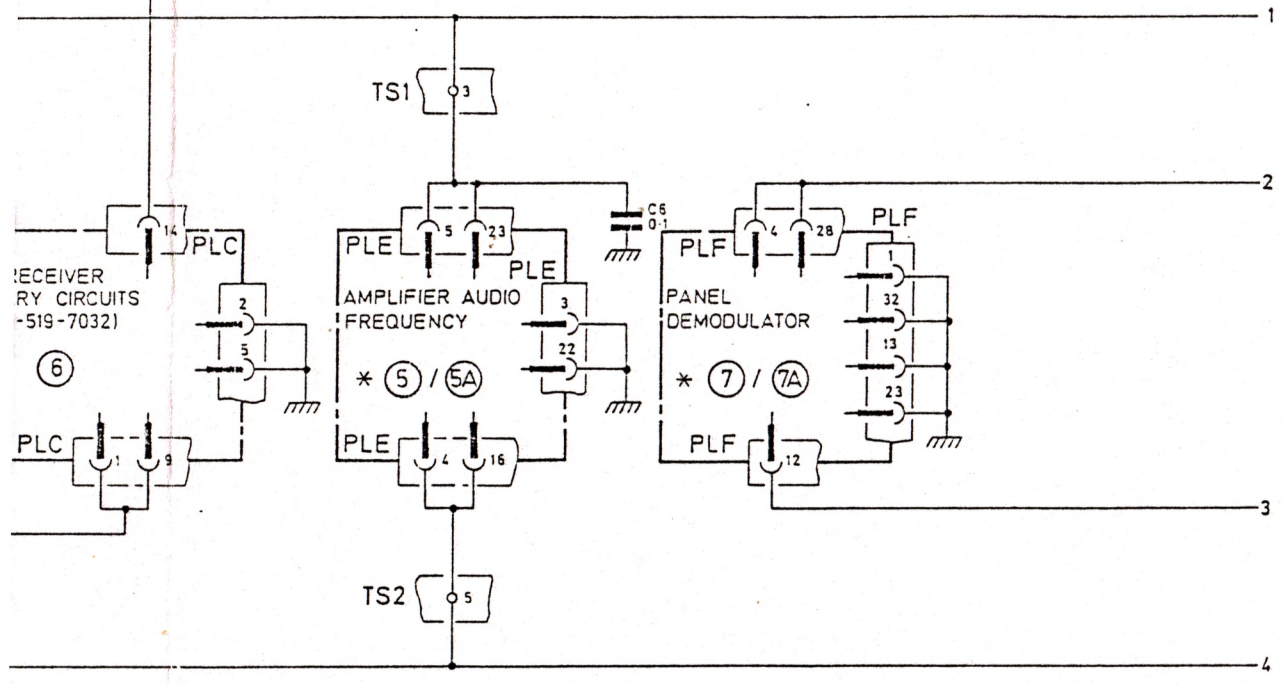
| | | |

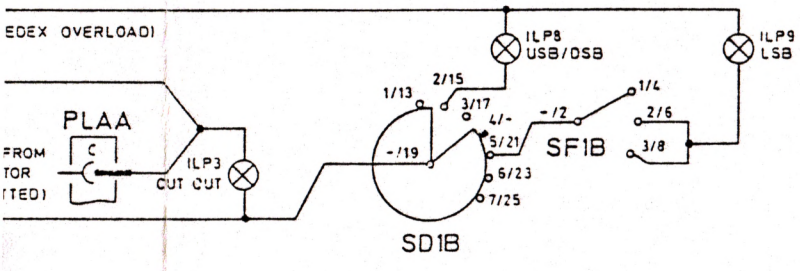


RLB
BASE VIEW

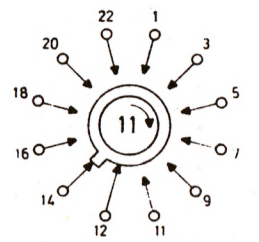


PLAA (PIN SIDE)
BASE VIEW

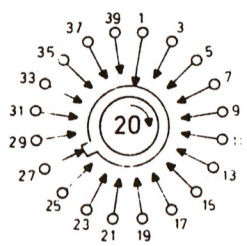




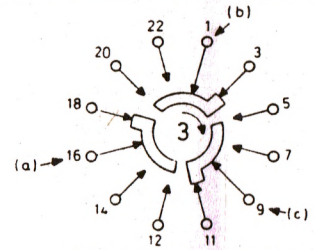
	RES
	CAP
	MISC



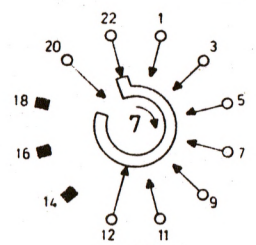
SA1F & SA2F



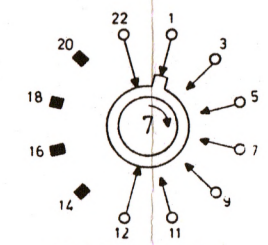
SB1F & SB2F



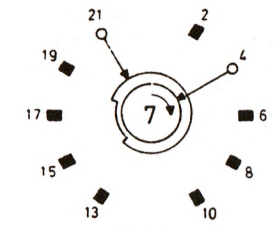
SC1F, SE1F & SF1F



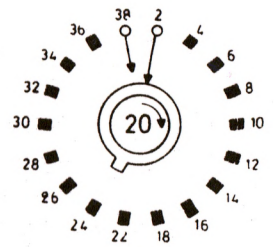
SD1F



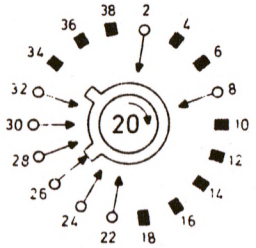
SD2F & SD3F



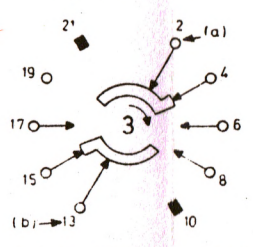
SD3B



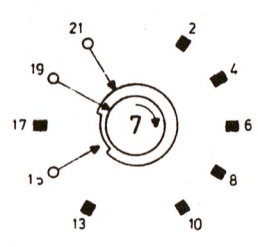
SB1B



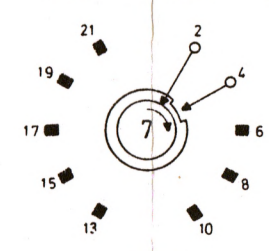
SB2B



SC1B, SE1B & SF1B

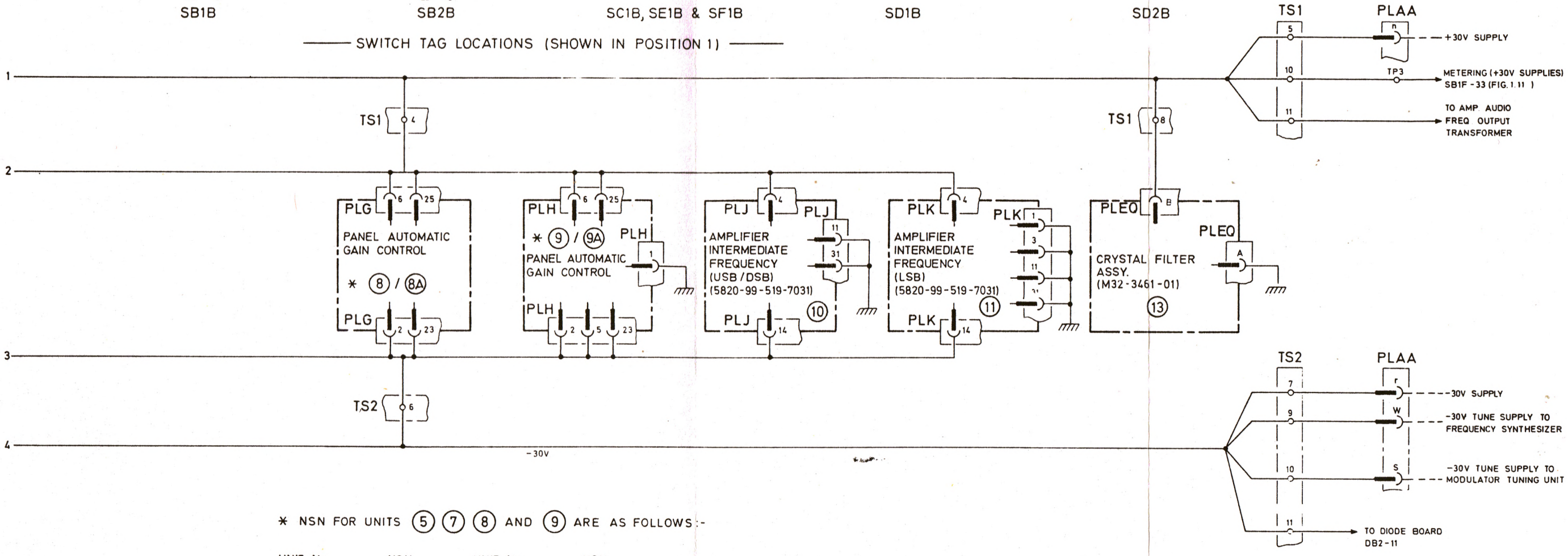


SD1B



SD2B

SWITCH TAG LOCATIONS (SHOWN IN POSITION 1)



* NSN FOR UNITS (5) (7) (8) AND (9) ARE AS FOLLOWS:-

UNIT No.	NSN	UNIT No.	NSN
(5)	5820-99-519-7030	(5A)	5820-99-758-9180
(7)	5820-99-519-7029	(7A)	5820-99-758-9179
(8)	5820-99-519-7028	(8A)	5820-99-758-9181
(9)	5820-99-519-7028	(9A)	5820-99-758-9181

NOTE FOR SWITCH ENGRAVING SEE FIG 1.12

MOD RECORD
1 2 3 4 5 6
7 8 9 10 11 12

RECEIVER RADIO FREQUENCY 5820-99-519-7019
SUB-ASSEMBLY 1 (POWER DISTRIBUTION) CIRCUIT DIAGRAM

FIG 1.13B

CHAPTER 2

TUNING UNIT RECEIVER 5820-99-519-7020

UNIT 2

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General Arrangement	5 - 9
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Overload Prevention Unit	13
R.F. Amplifier Assembly	14, 15
Oscillator Filter Assembly	16
Ledex Assembly	17, 18
Gearbox Assembly	19, 20
ELECTRICAL DESCRIPTION	
General Arrangement	21 - 30
R.F. INPUT FILTER ASSEMBLY	31 - 42
Antenna Input and Overload Prevention	31 - 36
Overload Prevention Unit	37 - 40
Input Filtering	41, 42
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GEARBOX ASSEMBLY	58

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Tuning Unit Receiver Component Layout	2.3
R.F. Input Filter Assembly Component Layout	2.4
R.F. Amplifier Assembly Component Layout	2.5
Oscillator Filter Assembly Component Layout	2.6
Overload Prevention Board Component Layout	2.7
Main Signal Flow Circuit Diagram	2.8A

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ILLUSTRATIONS (Cont'd)

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Servo and Range Control Circuit Diagram	2.8B
R.F. Amplifiers Circuit Diagram	2.8C
R.F. Input and Oscillator Filters Circuit Diagram	2.9D

CHAPTER 2

TUNING UNIT RECEIVER 5820-99-519-7020

UNIT 2

Introduction

1. The Tuning Unit Receiver accepts an r.f. input from the antenna over the frequency range 240 to 525 kHz and 1.0 to 27.9999 MHz and provides the final i.f. at 100 kHz for the two sideband channels.

2. Overload protection against high antenna voltage is provided and r.f. filtering is followed by two stages of r.f. amplification using six tuned circuits which are automatically controlled from the Synthesizer.

3. The first frequency change produces an i.f. of 1 MHz or 4 MHz, for signal frequencies below or above 8 MHz. A second frequency change translates the amplified 4 MHz i.f. to 1 MHz. The first or second 1 MHz i.f. is then amplified and mixed to produce the final i.f. at 100 kHz. Local oscillator frequencies are derived from the 1 MHz standard via the Synthesiser and the Frequency Offset Unit.

4. The Tuning Unit Receiver comprises units 19 to 25 inclusive, described in Chapter 3 to 9, plus the following identifiable sub-assemblies which are described in this chapter:-

(a) Overload Prevention Unit.

(b) R.F. Input Filter Assembly.

(c) R.F. Amplifier Assembly.

(d) Oscillator Filter Assembly.

(e) Filter Band-pass 5915-99-519-7021.

(f) Ledex Assembly.

(g) Gearbox Assembly.

PHYSICAL DESCRIPTION

General Arrangement

Figure 2.3

5. Unit 2 has an aluminium chassis secured to the Receiver chassis by four screws. Its size is 17.5 inches by 7.75 inches by 2.75 inches.

6. On the underside of the chassis there are the R.F. Input Filter, R.F. Amplifier and Oscillator Filter assemblies each of which contains six sets of inductors and trimming capacitors for all r.f. and oscillator filtering, together with the assoicated switch sections.

7. The switch sections of the three assemblies are coupled by insulated flexible couplings and driven by a Ledex motor mounted on a plate which fits on the end of the chassis. The filter assemblies can be removed individually by unsoldering leads as necessary, slackening the coupling grub screws and removing four retaining screws.

8. On the top of the chassis there are two 4-gang variable capacitors which tune the filter assemblies. The capacitors are driven from a gearbox assembly on which is mounted a servo motor and a helical potentiometer.

9. Units 19 to 23 are printed wiring boards which plug into 16-way edge connectors on the chassis. They are surrounded by aluminium screens. The F.O.S.U. Wideband Amplifier, unit 24, is a wired-in board which fits on the front plate and also has an aluminium screen. The 1 MHz Limiter Board, unit 25, is wired-in and mounted on a plate which is hinged to provide access to the 4 MHz crystal filter underneath.

R.F. Input Filter Assembly — Figure 2.4

10. The assembly consists of two trays, each containing coils and trimming capacitors for three frequency ranges. The trays are on either side of the frequency range-selecting switch, and top, bottom, side and end plates completely enclose the unit. The plates are easily removed for access to the range switch and circuit components.

11. The unit fits underneath the Tuning Unit chassis between the Ledex assembly and the R.F. Amplifier assembly, flexible couplings at each end of the switch shaft providing the mechanical linkage. The switch shaft has a red painted flat on one end to facilitate alignment with corresponding range markings on the end plate.

12. Lead-through terminals on the end plates are provided for input and output connections to the filter section, and three pairs of terminals on the top provide connections to the three sections of the ganged tuning capacitor.

Overload Prevention Unit — Figures 2.4, 2.7

13. A bracket on one end of the R.F. Input Filter Assembly Supports the Overload Prevention Board and its associated components, including plug-in relay RLA and AERIAL IN, AERIAL OUT coaxial M.U.S.A. type plugs.

R.F. Amplifier Assembly — Figure 2.5

14. Construction is similar to the R.F. Input Filter Assembly and the switch shaft is marked in the same way.

15. Each tray contains one valve and its associated circuitry, also the coils and trimming capacitors for three frequency ranges. The valves, mounted partially inside the unit, are fitted with valve cans with cooling liners to reduce their running temperature.

Oscillator Filter Assembly — Figure 2.6

16. Construction is similar to the R.F. Input Filter Assembly and the switch shaft is marked in the same way. The trays also have screens to provide isolation between the coupled tuned circuits and to isolate the r.f. section from the local oscillator filter section.

Ledex Assembly — Figure 2.3

17. The assembly is mounted on a bracket and comprises a Ledex motor with two homing wafers and associated components. An extension shaft enables the motor to drive the Tuning Unit filters via a flexible coupling.

18. An 18-way plug attached to the bracket carries the Ledex motor supply and range control voltages to the homing wafers. A red dot is painted on the flat of the drive shaft. This indicates Range 1 position when the dot is on the same side of the motor as the wire guard protecting the step contact.

Gearbox Assembly — Figure 2.3

19. The gearbox assembly comprises a gear train, providing one drive from the servo motor through a 7:1 reduction to the helical potentiometer, and another through a 20:1 reduction to the drive spindle of the main tuning capacitor. The helical potentiometer is a ten-turn potentiometer. For the full ten turns the main tuning capacitor turns through 180 degrees.

20. The gear train is fitted with end stops which restrict the rotation of the tuning capacitor to 177 degrees. This prevents the end stops of the potentiometer being damaged. The gear train stops are not adjustable and the potentiometer must be set correctly in relation to them.

ELECTRICAL DESCRIPTION

General Arrangement — Figures 2.2, 2.8 A to D

21. Antenna input arrangements are suitable for common antenna systems where a number of Receivers are connected in series on a coaxial cable from a single antenna.

22. The overload prevention circuit is fed with a proportion of the antenna input voltage and when this exceeds approximately 5 V it operates a relay which short-circuits the antenna input and output plugs and disconnects them from the tuned circuits, thus preventing damage in the Receiver.

23. The R.F. Input Filter comprises three tuned circuits for each range, interposed between the antenna and the first amplifier valve. The frequency ranges for reception are shown in Table 2.1.

Table 2.1 — Frequency Ranges

Range	Frequency
1	240 to 525 kHz
2	1.0 to 1.9999 MHz
3	2.0 to 3.9999 MHz
4	4.0 to 7.9999 MHz
5	8.0 to 15.9999 MHz
6	16.0 to 27.9999 MHz

24. The two stages of r.f. amplification employ valves to give high performance with high-level adjacent signals. A single tuned circuit between the two valve amplifiers, in conjunction with a coupled pair after the second valve, provides further rejection to off-tune signals before the mixer.

25. The filtered r.f. output is applied to the First Frequency Changer, unit 21. The range switch controls diode switches so that on ranges 1 to 4 it is applied to the 1 MHz i.f. frequency changer which produces a first i.f. of 1 MHz, and on ranges 5 and 6 it is applied to the 4 MHz i.f. frequency changer to produce a first i.f. of 4 MHz. The local oscillator frequency is derived from the Synthesiser, in conjunction with the Frequency Offset Unit, then amplified and filtered to reduce out of band noise and spurious signals.

26. The 1 MHz first i.f. for ranges 1 to 4 is routed directly to the 1 MHz I.F. Amplifier, unit 20.

27. The 4 MHz first i.f. for ranges 5 and 6 is passed through a crystal 'roofing' filter, amplified and applied to a second frequency changer where it is mixed with a 3 MHz signal to produce a second i.f. of 1 MHz. The 3 MHz signal for this mixer is derived from the 1 MHz Standard by multiplication and filtering in the F.O.S.U.

28. The 1 MHz first or second i.f. is amplified with some further filtering before being applied to the third frequency changer where it is mixed with a 1.1 MHz signal to produce the final i.f. of 100 kHz. This is fed to the Crystal Filter Assembly, unit 12. The 1.1 MHz signal for the third frequency changer is produced by mixing the 1 MHz Standard with 100 kHz from the Frequency Synthesiser. Alternatively, for fine tuning, the 100 kHz is derived from the 100 kHz crystal oscillator which can be pulled by $\pm$ 50 Hz in 10 Hz steps by the FINE TUNING Switch which applies the appropriate d.c. voltage to a varactor diode in series with the crystal. When the switch is set to the 0 position the 100 kHz from the Frequency Synthesiser is switched into operation to maintain the frequency stability of the Standard.

29. Test facilities are incorporated which, with the front panel meter and METERING switch, enable 4 MHz or 1 MHz signals to be injected at appropriate points in the amplifiers for monitoring and fault finding.

30. Figure 2.2 is a simplified circuit of the Tuning Unit filters, showing the six signal frequency tuned circuits and the two oscillator frequency tuned circuits of one range. The capacitors are ganged and servo tuned over the frequency swing required of the range, normally 2:1. There are six ranges with six sets of coils, and the capacitors are switched to the coils of the range in use. The coils on other ranges are shorted out.

R.F. INPUT FILTER ASSEMBLY

Antenna Input and Overload Prevention

Figure 2.1

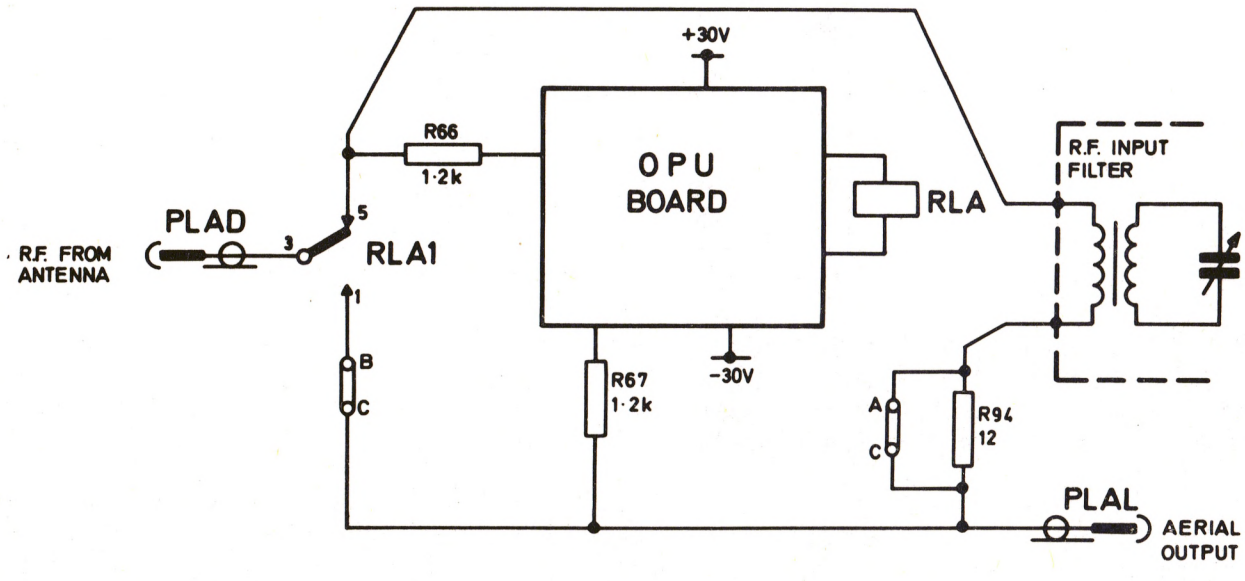


Fig 2.1 AERIAL INPUT CIRCUIT

31. Separate antenna input and antenna output plugs, with the coupling winding of the first tuned circuit connected between them, enable a number of Receivers to be supplied from a single antenna by connecting them in series on a 75 ohm coaxial feeder. When not used in a common antenna system the antenna output plug is fitted with a terminating socket which is either short-circuited or, in certain circumstances, fitted with a low resistance. (See Paragraph 36).

32. When used in a common antenna system terminals B, C and A, C should be linked. When the Receiver is switched off or an overload occurs RLA is de-energised, providing a short-circuit path between PLAD and PLAL and disconnecting the input coil from PLAD. Thus, no attenuation is inserted in the antenna feeder to the other Receivers.

33. With the Receiver switched on RLA is energised and RLA1 connects the input coupling winding between PLAD and PLAL. The input coupling presents an impedance of approximately 75 ohms on-tune and low impedance off-tune. The voltage across the input winding is also applied, via R66 and R67, to the Overload Prevention Unit. This contains a trigger circuit which operates when the antenna input voltage exceeds about 5 V and de-energises RLA. (See Paragraphs 37-40.)

34. Under common antenna working the O.P.U. gives protection only against high voltages on-tune, since off-tune the input impedance is low and excessive current could flow in the coil without producing sufficient voltage to operate the cutout. Since the common antenna feeder cable is finally terminated in 75 ohms, antenna voltages causing currents greater than 0.5 A are extremely unlikely. The antenna input windings are designed to carry 0.5 A without any damage occuring.

35. When operating with a single Receiver per antenna, it is necessary to protect against high voltages off-tune and terminals B, C and A, C should be unlinked. The 12 ohm resistor R94 is then inserted between the coupling winding and the short-circuited antenna output plug PLAL. The voltage developed across R94 operates the O.P.U. trigger circuit before currents in excess of 0.5 A occur.

36. If the Receiver is required to remain in operation with high-level off-tune signals it is necessary to fit a terminating resistor in place of a short-circuit across PLAL. Its value is set, with R94, to limit the current to 0.5 A under appropriate conditions eg for antenna voltages up to 20 V the total series resistance required = 20 ÷ 0.5 = 40 ohms. The external resistor will slightly degrade the signal-to-noise performance of the Receiver.

Overload Prevention Unit — Figure 2.8A

37. If large voltages are induced in the antenna either by a nearby transmitter or by lightning, the Overload Prevention Unit operates and RLA is de-energised. RLA1 disconnects the antenna from the R.F. Input Filter and, in the case of common antenna working, connects the antenna input socket directly to the antenna output socket. RLA2 switches the front panel CUTOUT lamp on and mutes the receiver by removing an earth from Diode Board DB2 unit 17, where -30 V is applied via 17R2 to the Panel Automatic Gain Control. RLA is also de-energised to switch on the CUTOUT lamp if the +30 V or -30 V power supplies fail.

38. Approximately one-tenth of the voltage which appears across the coupling coil in the R.F. Input Filter is applied to the primary of T3. The signal appearing at the secondary of T3 is detected by the shunt rectifier MR8. The potential developed across R70 is applied to VT1 base; diode MR2 limits the peak voltages which can appear during overload conditions and therefore protects VT1.

39. Normally, VT1 is not conducting and VT2 is saturated so that RLA is energised. During overload conditions the voltage developed across R70 causes VT1 to conduct and reduce VT2 base current. VT2 collector voltage rises to forward bias MR9 and increase VT1 base current. Cumulative action drives VT1 to saturation and switches VT2 off to de-energise RLA which remains so until the supply is switched OFF and ON again or until, during Simplex operation, the O.P.U. is automatically reset.

40. Automatic resetting of the O.P.U. is provided by MR13, R74, C6. On SEND -30 V is applied via the Receiver mute line to PLAT-M and C6 is charged. On RECEIVE the mute line voltage falls to zero and allows C6 to discharge through R74. VT2 base then receives a positive pulse via MR13, VT2 starts to conduct, bistable action cuts off VT1 and RLA is energised.

Input Filtering — Figures 2.8A, D

41. On each frequency range the r.f. input is filtered by three coupled tuned circuits between the antenna input and the grid of the first valve. They provide a voltage gain of 8 to 9 dB to the on-tune signal and an attenuation, relative to this, of approximately 30 dB to signals 5% off-tune.

42. The r.f. filter comprises three tuned circuits with inductive coupling between them. For example on Range 1, L11 is coupled to L12 by the small coupling winding on L12 connected in series with L11. The circuits are tuned by three sections of the main servo-driven tuning capacitor, C17, C19 and C27. The input is applied via a coupling winding on L11 which presents an input impedance of about 75 ohms between the aerial input terminals. The output is taken from a tap on L13, at an impedance level of approximately 4 kohms, via C40 to the grid of r.f. amplifier V1 on the R.F. Amplifier Assembly.

R.F. AMPLIFIER ASSEMBLY — Figures 2.8A, C

43. The R.F. Amplifier Assembly carries the r.f. amplifiers V1, V2 which have a single tuned circuit switched between them on each range. The gain from the grid of V1 to that of V2 is 5 dB on Ranges 1-4 and 6 dB on Ranges 5 and 6. These are gains at the low-frequency ends of ranges; the gain tends to increase with frequency.

44. Except on Range 1 the tuned circuit between V1 and V2 is designed to give sufficient attenuation, at $2\frac{1}{2}\%$ off-tune, to reduce the grid-to-grid gain to less than unity. On Range 1 this degree of selectivity would degrade Receiver a.f. response, so selectivity is reduced.

45. The r.f. amplifier stages employ pentode valves. On Range 1 the anode load of V1 is the tuned circuit L14, C14, C58, C57 with R39, R40 controlling the Q of the circuit. On Range 2, L24 and its associated circuitry is switched to replace L14, and so on for Ranges 3 to 6. Each circuit is tuned by C57 which is one of four ganged tuning capacitors on top of the Tuning Unit.

46. The valve circuits are the same, except that the anode load of V2 is two coupled tuned circuits in the Oscillator Filter Assembly.

47. R.F. A.G.C. grid circuitry eg R29, R31, C47, is designed to have attack and decay time constants of the order of 1 millisecond, to provide fast acting A.G.C. and muting in the Receiver.

48. V1 and V2 currents are monitored by a common metering circuit connected to the decoupled cathode-resistors of each stage. With both valves at full gain the current through R35, R52, decoupled by C49 will provide a reading of approximately 70 μA on the front panel METERING meter.

OSCILLATOR FILTER ASSEMBLY

Figures 2.8A, B, C, D

49. The Oscillator Filter Assembly contains two separate filter sections, one for the r.f. signal path and the other for the local oscillator r.f. path to the First Frequency Changer Board, Unit 21. It also contains range switching arrangements for metering circuits and for further distribution of d.c. voltages for range switching.

50. The anode load of V2 in the r.f. amplifier is the coupling winding of each tuned circuit of the r.f. filter, so the main tuning capacitor is isolated from the d.c. supply voltage. The r.f. filter on each range is a coupled pair of tuned circuits which, with the single tuned circuit of the r.f. amplifier, gives the required band-pass response. It is designed to give approximately 10 dB voltage gain between the grid of the r.f. amplifier V2 and its own output, with a passband response flat with $\frac{1}{4}$ dB over $\pm$ 3 kHz and a rejection of $\pm$ $2\frac{1}{2}$% so that the signal level at the output is never greater than that at V2 grid.

51. The signal output from the r.f. filter is taken from a nominal 150 ohm tap on the second tuned circuit. There are two coaxial outputs, one for Ranges 1 to 4 and the other for Ranges 5 and 6, which are fed to the 16-way edge connector SKTM.

52. The local oscillator filter section is designed to give further rejection of unwanted spurious signals from the Frequency Offset Unit, unit 3, and gives an attenuation of approximately 25 dB at $\pm$ 5% off-tune.

53. The oscillator filter has six switch positions covering the frequency ranges 240 to 525 kHz and 1 to 27.9999 MHz. On Ranges 1 to 4 the oscillator tuned filter frequency is offset by 1 MHz higher than the signal frequency, and on Ranges 5 and 6 it is offset by 4 MHz higher than the signal frequency.

54. The oscillator filter is a coupled pair of tuned circuits having a kQ of 1, and inductive coupling via fixed inductors which are wound on iron dust cores. The filter is fed from the F.O.S.U. Wide-band Amplifier, unit 24, having an output impedance of 75 ohms which controls the Q of the input coil. The Q of the output coils is controlled by the 75 ohm input impedance of the wideband amplifier in unit 21, which the filter feeds.

55. On the end of the range switch, outside the Oscillator Filter Assembly, are two switch wafers. One wafer provides range indication by switching a voltage from a potential dividing network of resistors to the front panel meter. The other wafer switches d.c. range voltages to diode switch circuits in the Receiver via PLAS.

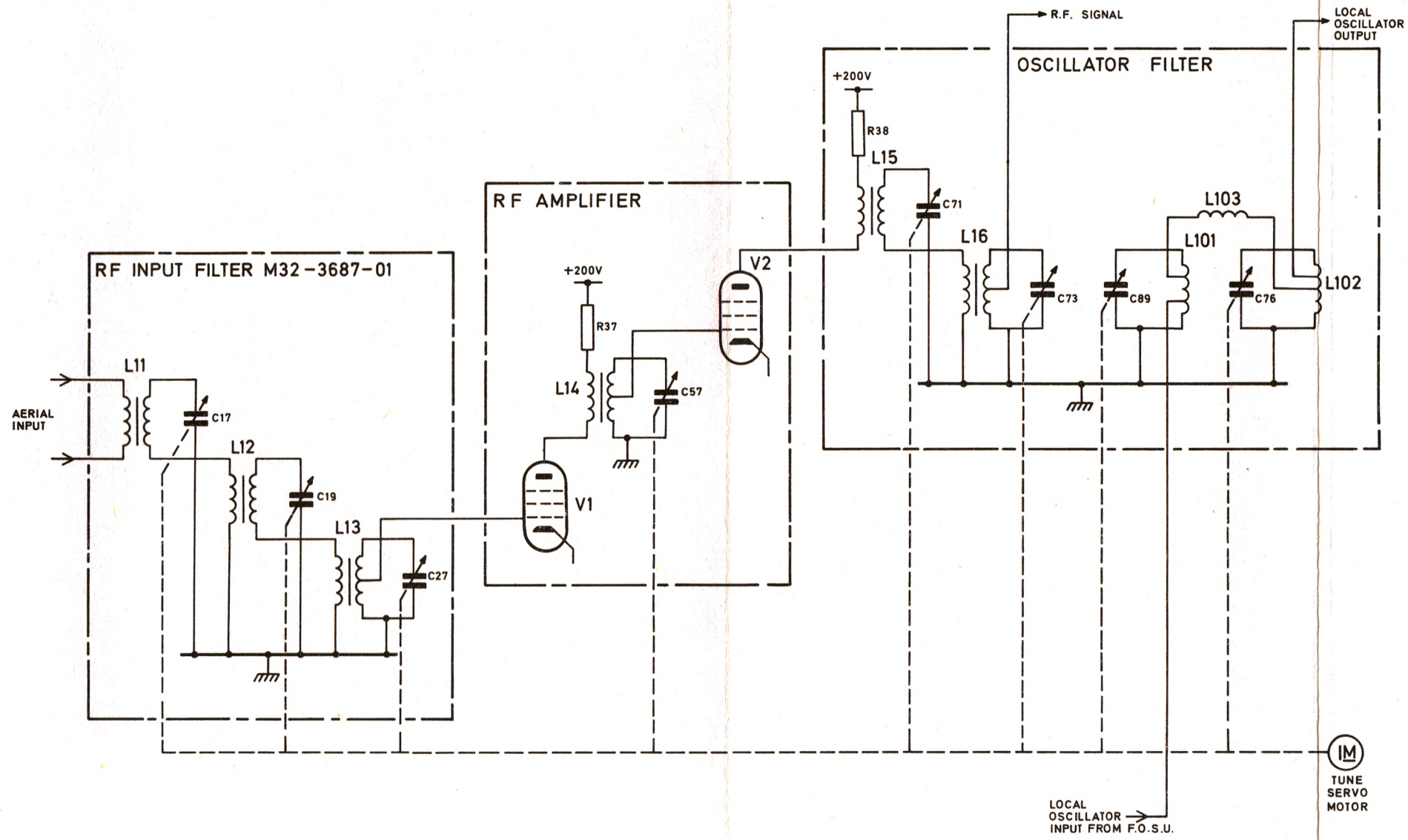
LEDEX ASSEMBLY

56. Ledex motor SA is supplied by +41 V via PLAC, A and controlled from the Synthesiser which applies -41 V to PLAC, C, D, E, F, H or J depending on the range in use. SA2F completes the circuit via solenoid operating contact SA1F to SA which drives SA2F to the open circuit position. -41 V spark quench return is provided at PLAC, U.

57. SA2B switches range control voltages to the Modulator Tuning Unit in Type 641. It is not used in Outfit CJM.

GEARBOX ASSEMBLY

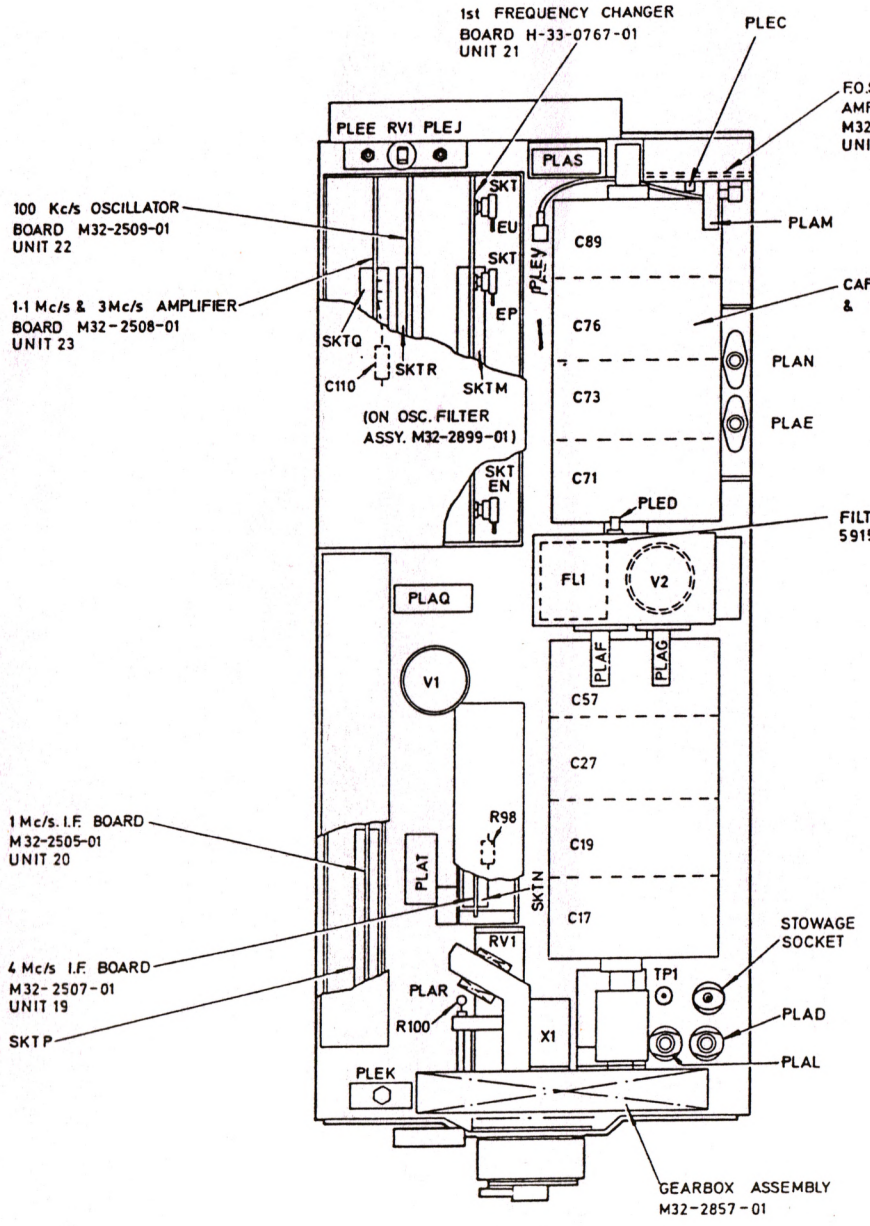
58. The gearbox is driven by two-phase, 400 Hz servo motor X1 which is supplied from Panel Servo Supply, unit 4 and controlled from the Synthesiser. The difference between the control voltage from the Synthesiser and that from the tune servo potentiometer R1 to R11 provides the input to unit 4. Compensating resistor R100, mounted on a small printed wiring board, is selected on test.



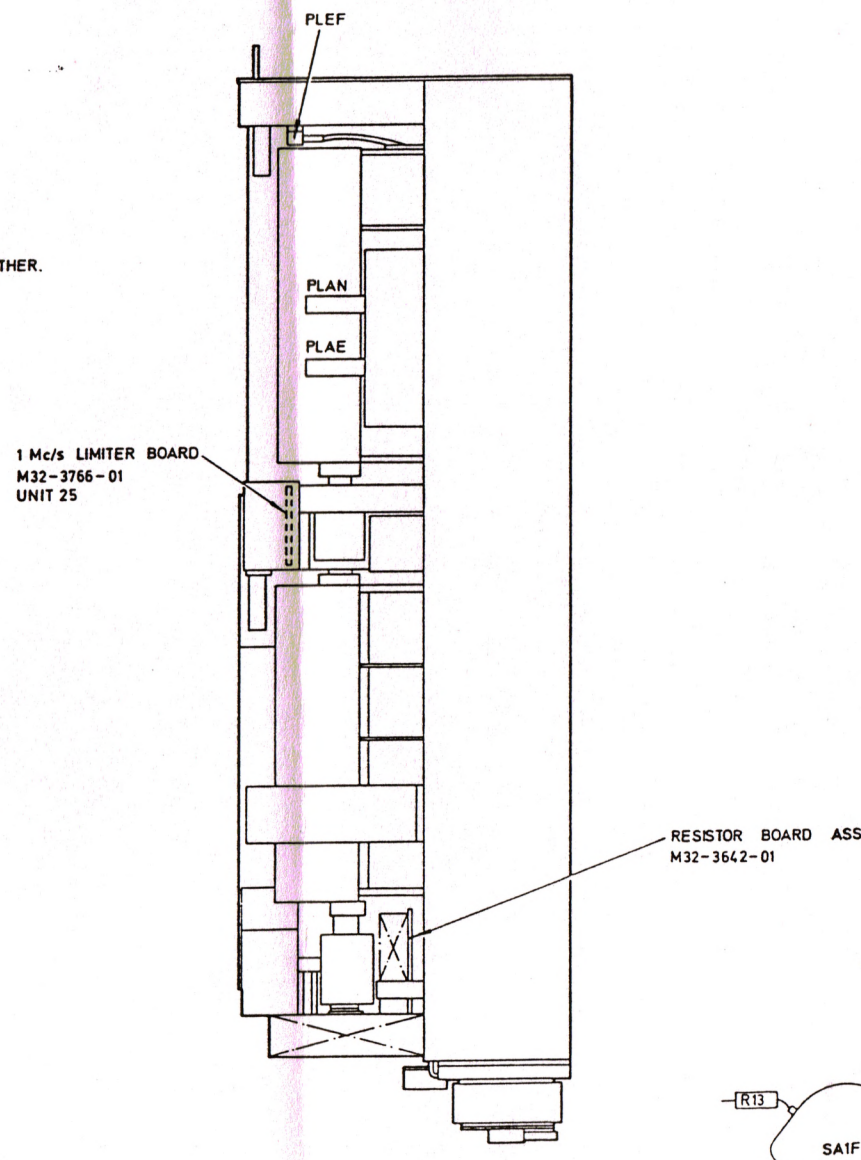
MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

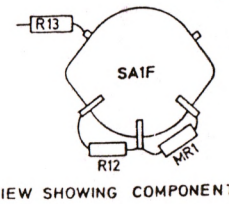
TUNING UNIT FILTERS
SIMPLIFIED CIRCUIT

FIG. 2·2

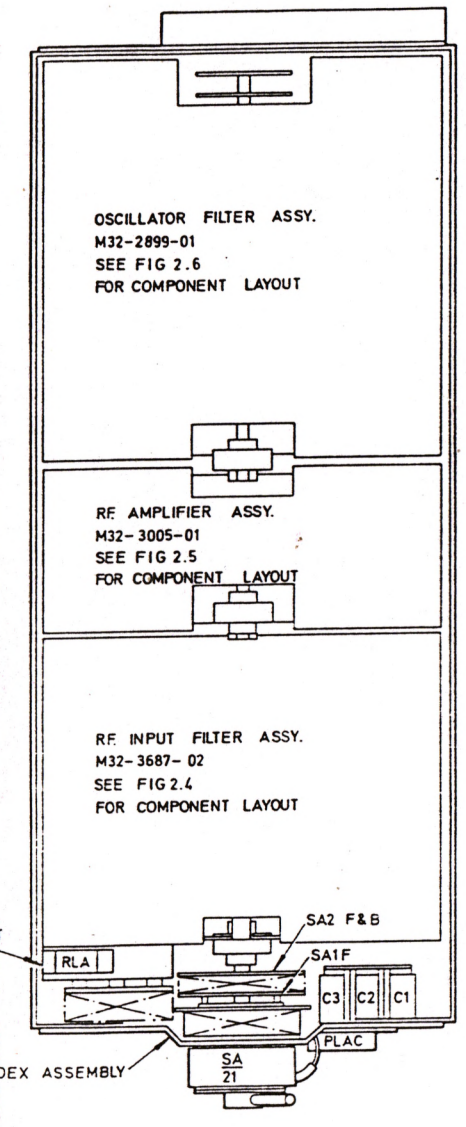


PLAN VIEW





VIEW SHOWING COMPONENTS AROUND SA1F



UNDER PLAN VIEW

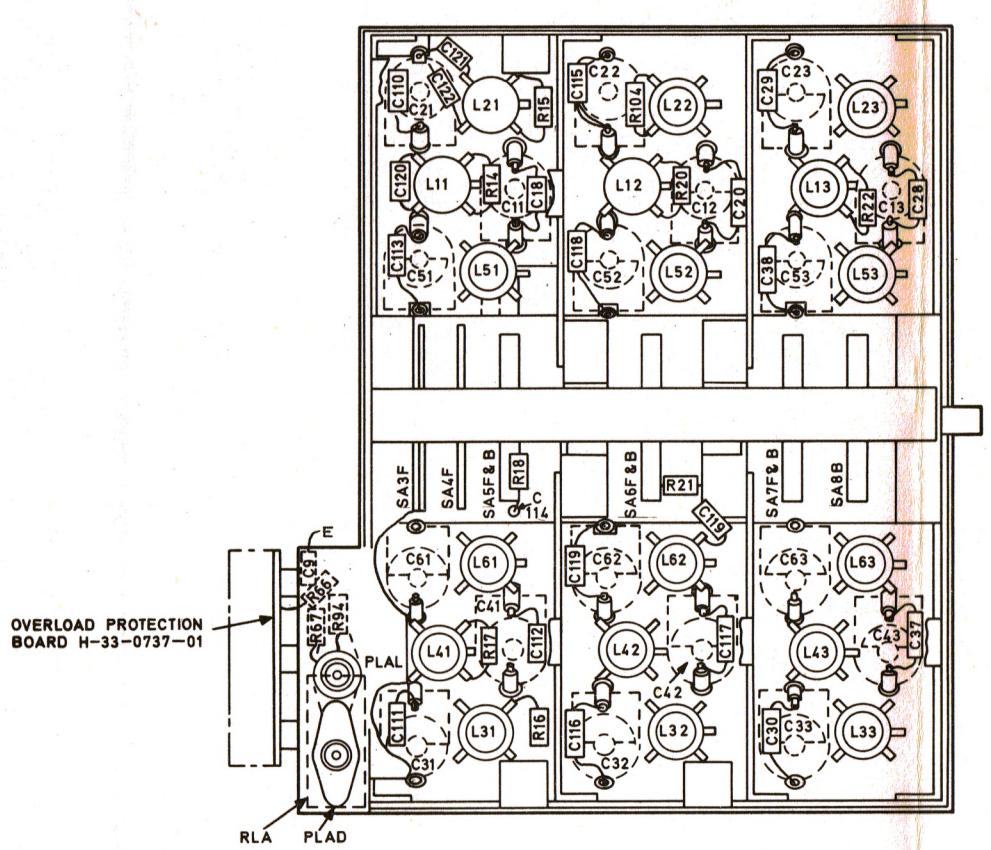
MOD RECORD					
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7	8	9	10	11	12

TUNING UNIT, RECEIVER 5820-99-519-7020

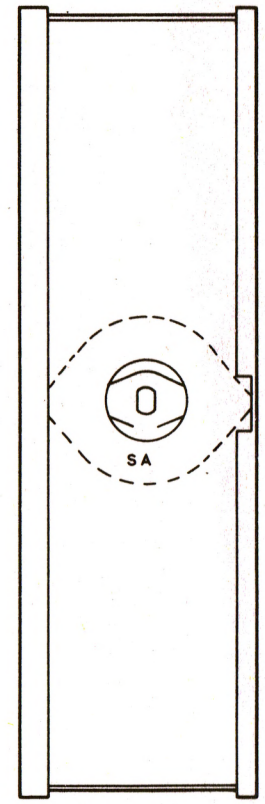
SUB ASSEMBLY 2

COMPONENT LAYOUT

FIG. 2·3



VIEW WITH BASE PLATE REMOVED

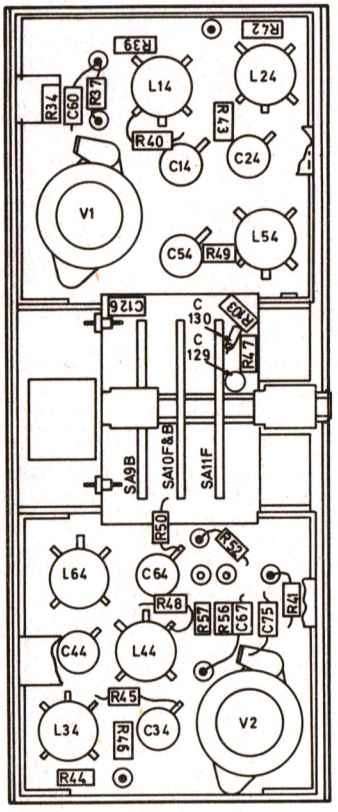


R.F. INPUT FILTER ASSY.

MOD RECORD					
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7	8	9	10	11	12

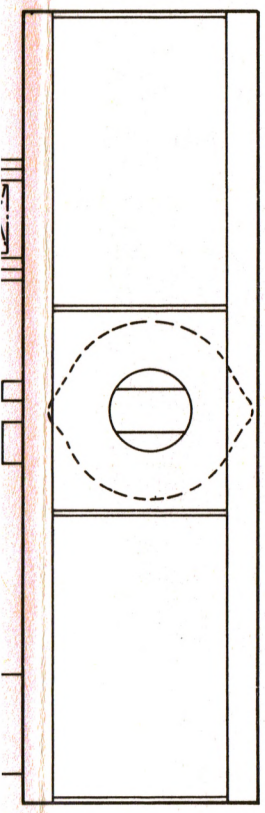
TUNING UNIT RECEIVER 5820-99-519-7020
SUB-ASSY 2 R.F. INPUT FILTER COMPONENT LAYOUT

FIG. 2-4

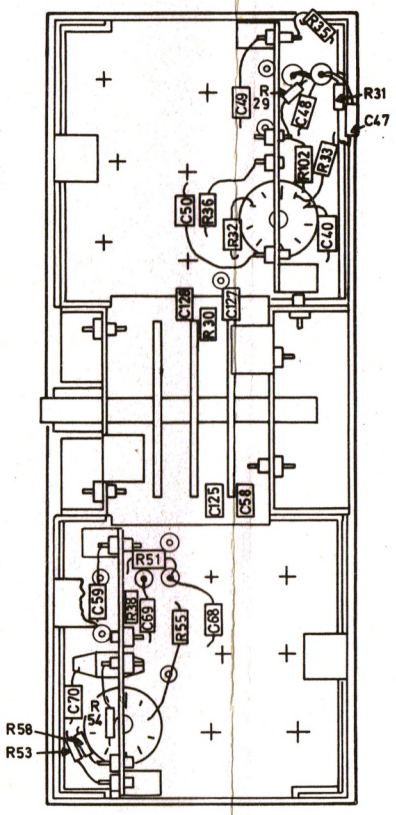


VIEW WITH COVER REMOVED





RF AMPLIFIER ASSY.



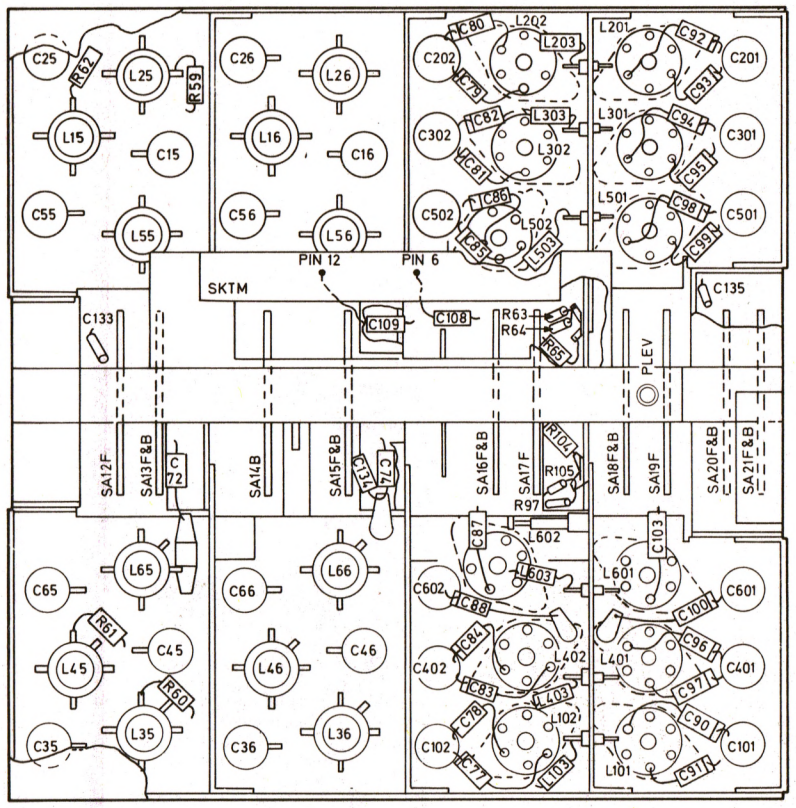
VIEW WITH COVER REMOVED

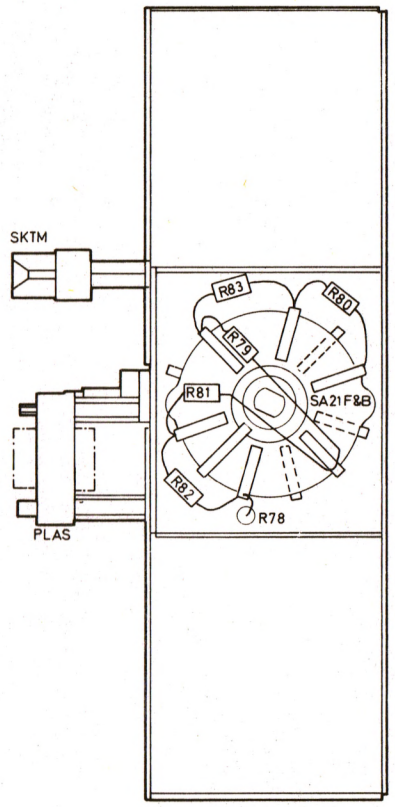
MOD RECORD					
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7	8	9	10	11	12

TUNING UNIT RECEIVER 5820-99-519-7020

SUB-ASSEMBLY 2 R.F. AMPLIFIER ASSY COMPONENT LAYOUT

FIG.2·5





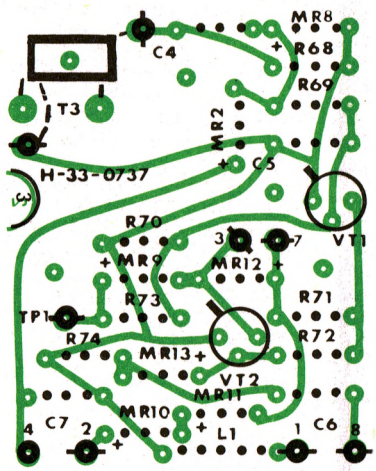
OSCILLATOR FILTER ASSEMBLY M32-2899-01

MOD RECORD					
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7	8	9	10	11	12

TUNING UNIT, RECEIVER **5820-99-519-7020**

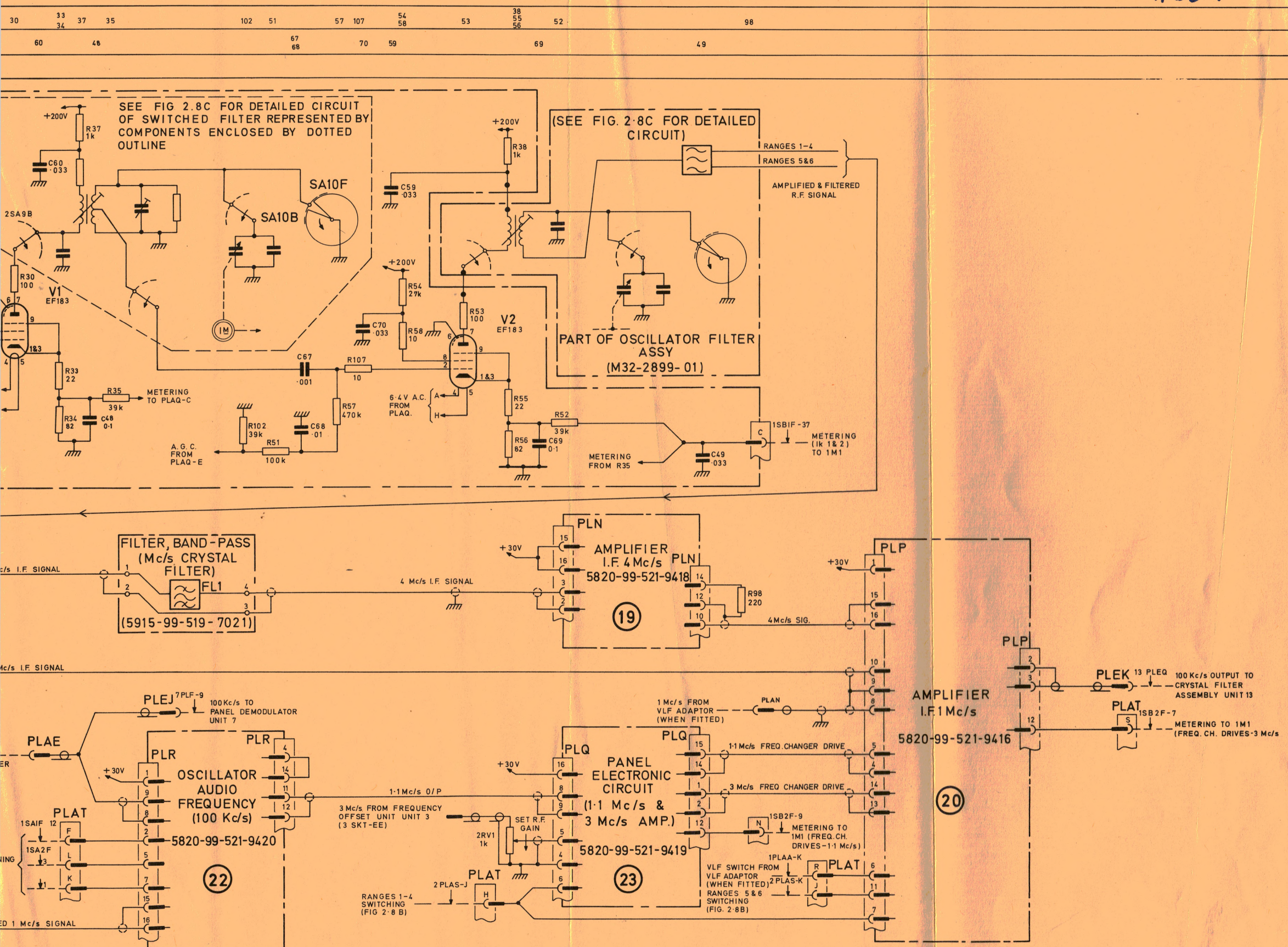
SUB-ASSEMBLY 2 OSCILLATOR FILTER ASSY. COMPONENT LAYOUT

FIG.2·6



H-33-0737(L) ISS3

FIG. 2.7 OVERLOAD PREVENTION BOARD COMPONENT LAYOUT



MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

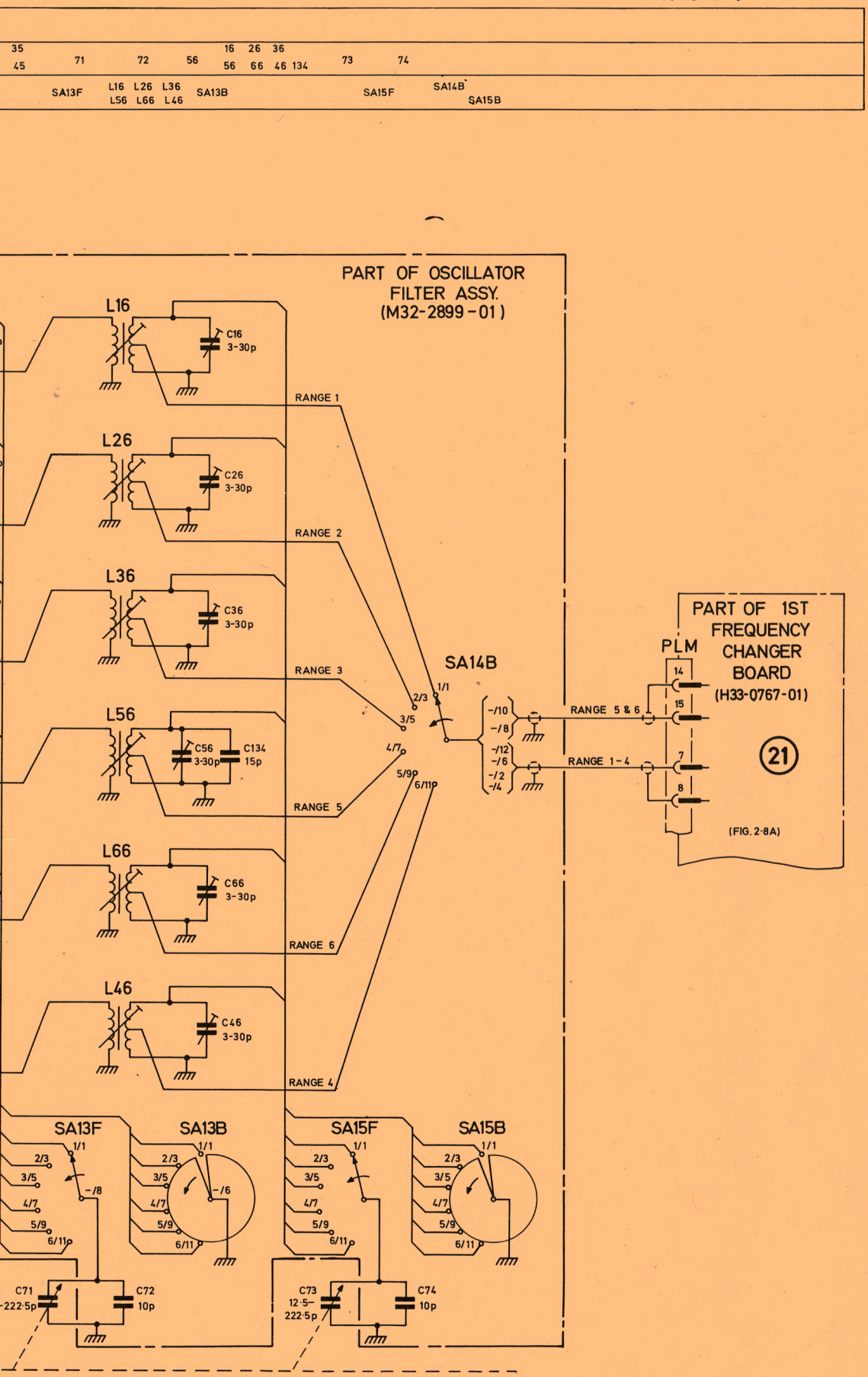
TUNING UNIT RECEIVER 5820-99-519-7020
SUB-ASSEMBLY 2 (MAIN SIGNAL FLOW) CIRCUIT DIAGRAM

FIG. 2·8A

| | | |

| | | |

| | | |



TUNING UNIT RECEIVER 5820-99-519-7020

SUB-ASSEMBLY 2 (R.F. AMPLIFIERS) CIRCUIT DIAGRAM

FIG. 2·8C

R.F. AMPLIFIER ASSEMBLY
(M32-3005-01)

RES	29 36 102 32,106 31 30 33 34 39 42 44 46 41 37 40 43 45 48 49 50 47 103 128 75 127 126 125 60 48 14 24 34 54 64 44 57 129 130 58 102 51 57 54 58 53 107 55 56 52 38 62 59 60 61
CAP	40 50 47 68 70 67 69 49 59 133 15 35
MISC	V1 SA9B L14 L24 L34 L54 L64 L44 SA10B SA11F SA10F V2 SA12F L15 L25 L35 L55 L65 L45

B.R. 4147 (5) A
Original Amdt 1

| | | |

| | | |

CHAPTER 3

FIRST FREQUENCY CHANGER BOARD

5998-99-016-0633

UNIT 21

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Physical Description	4, 5
ELECTRICAL DESCRIPTION	6 - 16
Test Facilities	15, 16

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First Frequency Changer Block Diagram	3.1
First Frequency Changer Component Layout	3.2
First Frequency Changer Circuit Diagram	3.3

CHAPTER 3

FIRST FREQUENCY CHANGER BOARD

5998-99-016-0633

UNIT 21

Introduction

Figure 3.1

1. The First Frequency Changer Board accepts inputs at signal frequency and first oscillator frequency from the Oscillator Filter Assembly M32-2899-01 and by amplification and mixing converts them to the first i.f. of 1 MHz on ranges 1 to 4 or 4 MHz on ranges 5 and 6.

2. On ranges 1 to 4 the Signal input at PLM7, 8 is applied to the 1 MHz I.F. Frequency Changer MR3 to MR6. On ranges 5 and 6 the signal input at PLM 15, 14 is applied to the 4 MHz I.F. Frequency Changer MR7 to MR10. The first oscillator frequency at PLM1 is amplified by VT1, VT2 and routed to the appropriate frequency changer by diode switches MR1, MR2 which are controlled by the range switch.

3. The 1 MHz i.f. output from PLEP is fed to the 1 MHz I.F. Amplifier. The 4 MHz i.f. output is amplified by VT3 and fed to the 4 MHz crystal filter via PLEN.

Physical Description

Figure 3.2

4. Unit 21 is a plug-in printed wiring board 6.4 inches by 2.5 inches. It is in a metal screening box at the front end of unit 2 and access is gained by removing the cover. Slotted guides assist location of the board and dowels on the printed-wiring side prevent it being inserted in the wrong position.

5. Four preset potentiometers, adjusted during initial setting-up, are mounted on the board. Six test points are provided on the component side. Points A and B are used for testing during manufacture.

ELECTRICAL DESCRIPTION

Figure 3.3

6. The First Oscillator r.f. input at PLM1 is applied to the base of common emitter amplifier VT1. The base voltage of VT1 is set by potential divider R1, R2 and the emitter current is controlled by the base voltage in conjunction with R6, R7. R6 provides negative feedback and R39 provides a feedback path which improves frequency response at the higher end of the frequency band.

7. VT1 is coupled to a second amplifier stage VT2 via C5. The d.c. conditions of VT2 are set in the same manner as VT1. A.C. negative feedback is used to counteract the falling off in performance at high frequencies and to stabilise the gain of the amplifier at low frequencies.

8. R13 provides current feedback whilst voltage feedback from collector to base is provided by C6, R10. As the feedback is reduced, the input impedance of VT2 and therefore the load on VT1 increases. The gain of VT2 rises in sympathy. The +30 V d.c. supply is decoupled by L1, R4 and C2 for VT1 and R11, C9 and C10 for VT2.

9. VT2 output is coupled by C8 to one of the frequency changers via diode switches MR7, MR2. The frequency changer in use depends on the position of the range switch. Ranges 1 to 4 select the 1 MHz i.f. and ranges 5 and 6 select the 4 MHz i.f.

10. The 1 MHz output is direct and the 4 MHz output is applied to amplifier VT3 but the action of each frequency changer is the same. Only the 4 MHz i.f. frequency changer will be described.

11. The first oscillator frequency output of VT2 is fed via diode switch MR1 and transformer T4 to the 4 MHz i.f. frequency changer where it is mixed with the incoming r.f. signal from the tuning unit circuits to produce an i.f. output of 4 MHz.

12. MR1 may be considered as one arm of a two-way switch. Its anode is connected via R15 to earth. In the 'off' condition, with no connection to PLM12, MR1 cathode is connected to +30 V via R23, R24, R25 and MR1 is reverse biased. In the 'on' condition, -30 V is applied to PLM12 and MR1 conducts. Current is then controlled by R15, R25, R24.

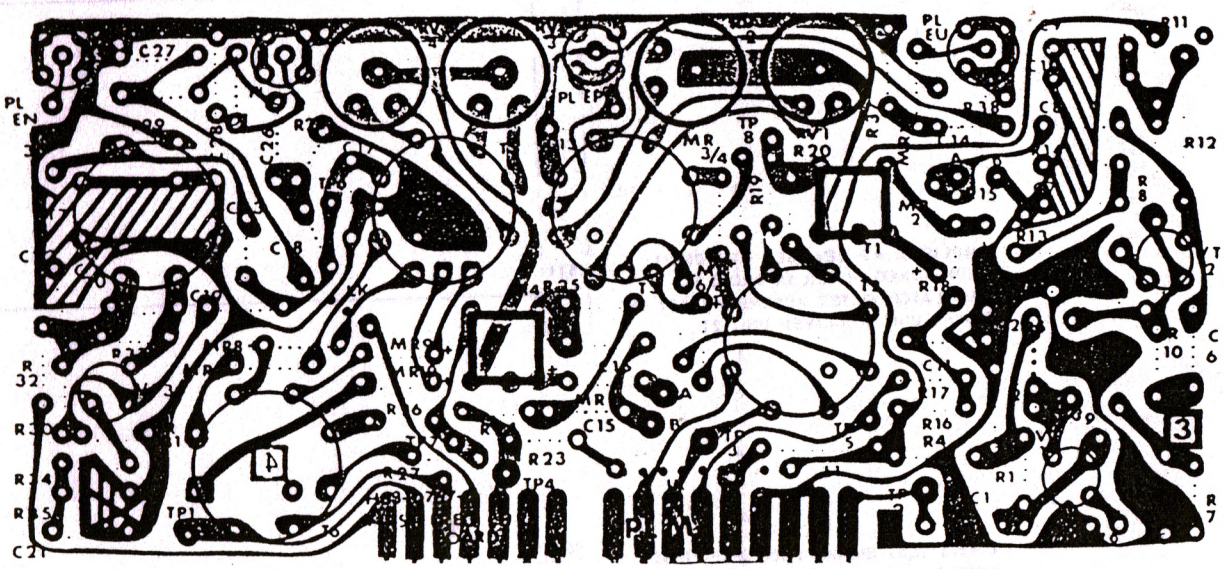
13. The r.f. signal at PLM15, 14 is applied to input transformer T6. The secondary windings of T6 are connected to mixer circuit MR7 to MR10. This is a double balanced modulator. MR7 and MR8 are conducting on one half cycle of the first oscillator frequency and MR9 and MR10 on the other half cycle. Thus, the route for the signal frequency from T6 to T5 alternates between the two paths at a rate determined by the first oscillator frequency. The two paths provide 180 degrees phase difference so that an output at the difference frequency of 4 MHz is obtained at T5, which is tuned by C17 to this frequency. RV3 and RV4 are used to balance the amount of drive frequency appearing at the output. R26 and R27 set the drive source resistance and assist in obtaining a clean switching action.

14. The 4 MHz output from T5 secondary is coupled by C19 to the base of VT3. The d.c. conditions of VT3 are set in a similar manner to those of VT1. Negative feedback is provided by R34. VT3 provides a small amount of gain for the 4 MHz i.f. output and a source impedance of approximately 400 ohms for the crystal filter through which the 4 MHz signal is fed. Part of this impedance is supplied by the turns ratio of T7 and R33, and is padded out to the correct value by R36. Amplifier VT3 is neutralised by C23 against adverse effects which might interfere with the filter performance.

Test Facilities

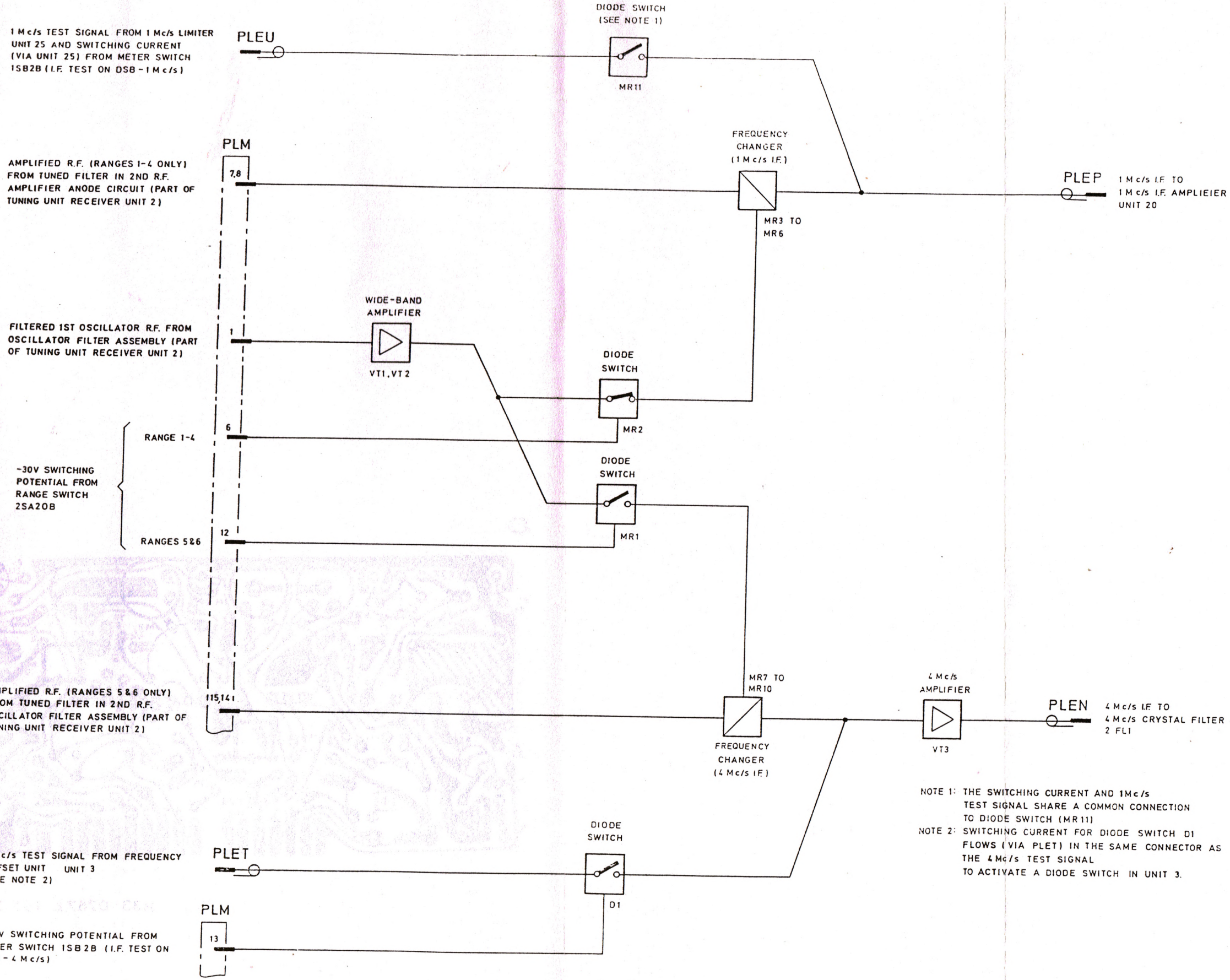
15. A fixed portion of the 4 MHz signal from the Frequency Offset Unit is available at PLET for test purposes. A potential of -30 V applied to PLM13 passes via R29 and PLET and activates a diode switch at source

16. A 1 MHz test signal and switching current from the 1 MHz Limiter Board, unit 25, may be switched to PLEU to switch on MR11. This provides an output at PLEP via C14.



H33 0767L 1SS 3

FIG. 3.2 FIRST FREQUENCY CHANGER BOARD COMPONENT LAYOUT



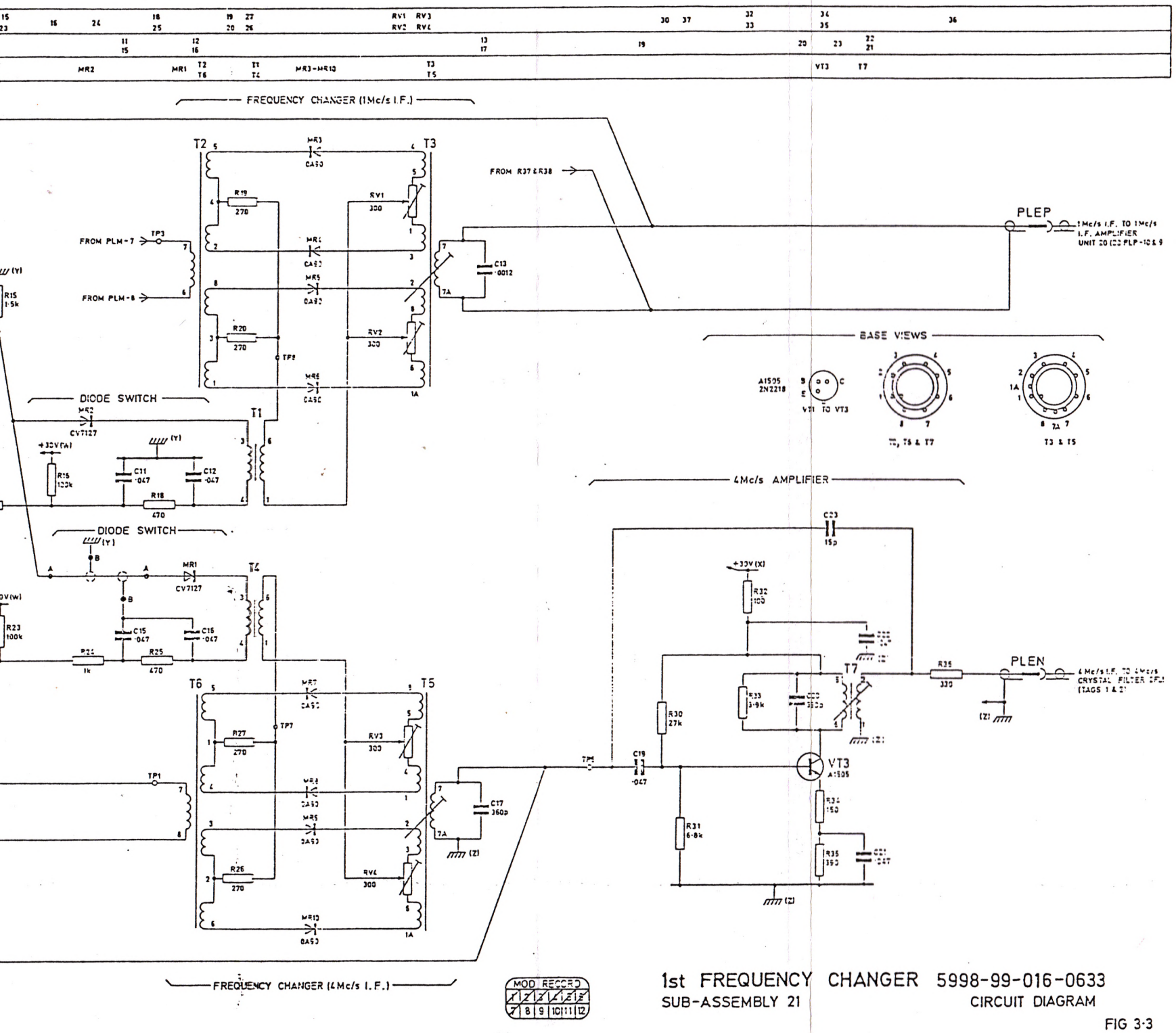
PANEL ELECTRONIC (1st. FREQ. CHANGER) 5998-99-016-0633

SUB-ASSEMBLY 21

BLOCK DIAGRAM

FIG. 3·1

B.R. 4147 (5) A
Amdt. 10, 5.93



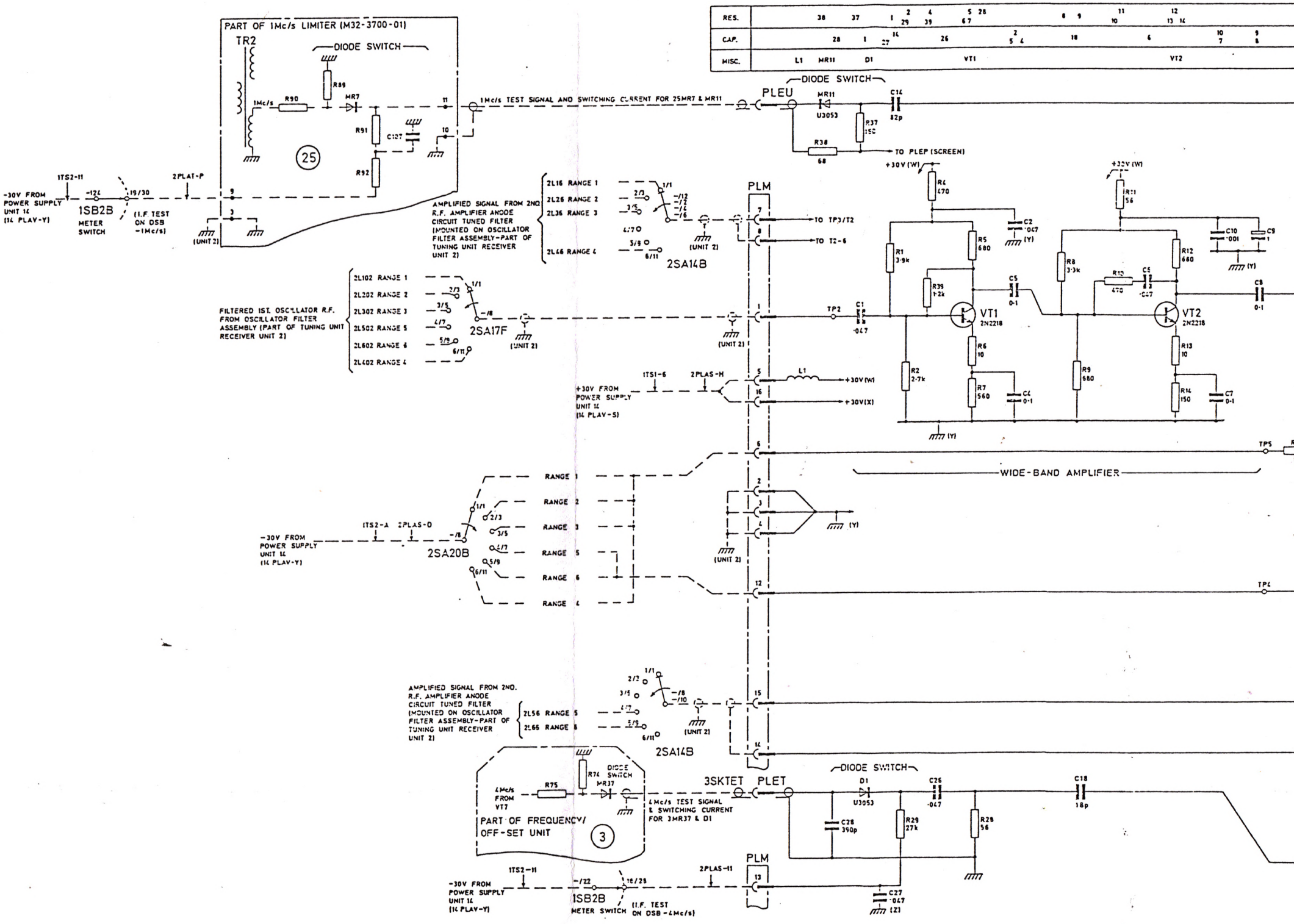
MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

1st FREQUENCY CHANGER 5998-99-016-0633

SUB-ASSEMBLY 21 CIRCUIT DIAGRAM

FIG 3·3


PART OF 1Mc/s LIMITER (M32-3700-01)
TR2
DIODE SWITCH
R89
R90
MR7
R91
C107
R92
25
1Mc/s TEST SIGNAL AND SWITCHING CURRENT FOR 2SMR7 & MR11
PLEU
MR11
U3053
C14
82p
R37
15C
R38
68
TO PLEP (SCREEN)
DIODE SWITCH
+30V (W)
R4
470
R1
3·9k
R5
680
C2
·047
(Y)
R39
1·2k
C5
0·1
VT1
2N2218
R6
10
R2
2·7k
R7
560
C4
0·1
R8
3·9k
R10
470
C3
·047
R12
680
C10
·001
C9
1
C8
0·1
VT2
2N2218
R13
10
R9
680
R14
150
C7
0·1
+32V (W)
R11
56
-30V FROM POWER SUPPLY UNIT 1L (1L PLAV-Y)
1TS2-11
-12/
19/30
1SB2B
METER SWITCH
(I.F TEST ON OSB -1Mc/s)
2PLAT-P
(UNIT 2)
AMPLIFIED SIGNAL FROM 2ND. R.F. AMPLIFIER ANODE CIRCUIT TUNED FILTER (MOUNTED ON OSCILLATOR FILTER ASSEMBLY-PART OF TUNING UNIT RECEIVER UNIT 2)
2L16 RANGE 1
2L26 RANGE 2
2L36 RANGE 3
2L46 RANGE 4
2SA14B
PLM
TO TP3/T2
TO T2-6
TP2
C1
·047
FILTERED 1ST. OSCILLATOR R.F. FROM OSCILLATOR FILTER ASSEMBLY (PART OF TUNING UNIT RECEIVER UNIT 2)
2L102 RANGE 1
2L202 RANGE 2
2L302 RANGE 3
2L502 RANGE 5
2L602 RANGE 6
2L402 RANGE 4
2SA17F
1TS1-6
2PLAS-H
L1
+30V (W)
+30V (X)
+30V FROM POWER SUPPLY UNIT 1L (1L PLAV-S)
TP5
WIDE-BAND AMPLIFIER
TP4
-30V FROM POWER SUPPLY UNIT 1L (1L PLAV-Y)
1TS2-A
2PLAS-D
2SA20B
RANGE 1
RANGE 2
RANGE 3
RANGE 5
RANGE 6
RANGE 4
AMPLIFIED SIGNAL FROM 2ND. R.F. AMPLIFIER ANODE CIRCUIT TUNED FILTER (MOUNTED ON OSCILLATOR FILTER ASSEMBLY-PART OF TUNING UNIT RECEIVER UNIT 2)
2L56 RANGE 5
2L66 RANGE 6
2SA14B
4Mc/s FROM VT7
R75
R74
DIODE SWITCH
MR37
PART OF FREQUENCY/ OFF-SET UNIT
3
4Mc/s TEST SIGNAL & SWITCHING CURRENT FOR 3MR37 & D1
3SKTET
PLET
DIODE SWITCH
D1
U3053
C26
·047
C18
18p
C28
350p
R29
27k
R28
56
C27
·047
(Z)
PLM
2PLAS-11
1TS2-11
-22
16/28
1SB2B
METER SWITCH
(I.F. TEST ON OSB -4Mc/s)
-30V FROM POWER SUPPLY UNIT 1L (1L PLAV-Y)

CHAPTER 4

4 MHZ I.F. AMPLIFIER 5820-99-521-9418

UNIT 19

CONTENTS LIST

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Introduction	1, 2
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Electrical Description	4 - 6

ILLUSTRATIONS

	Figure No
4 MHz I.F. Amplifier Component Layout	4.1
4 MHz I.F. Amplifier Circuit Diagram	4.2

CHAPTER 4

4 MHZ I.F. AMPLIFIER 5820-99-521-9418

UNIT 19

Introduction

1. The 4 MHz I.F. Amplifier is in use when the range switch is on ranges 5 or 6. It amplifies the 4 MHz output from the crystal filter sufficiently to provide a suitable signal-to-noise ratio at the second frequency changer stage. The output from this board is applied directly to the second frequency changer which is on the 1 MHz I.F. Board, unit 20.

2. The amplifier is frequency selective and is centred on the first i.f. of 4 MHz. Sufficient selectivity has been incorporated to back up the preceding crystal filter off-channel performance.

Physical Description

Figure 4.1

3. Unit 19 is a plug-in printed wiring board 3.6 inches by 2.6 inches. It is in a metal screening box and access is gained by removing the cover. Slotted guides assist location of the board into its socket. Three test points are provided on the component side. Points A and B are used for testing during manufacture.

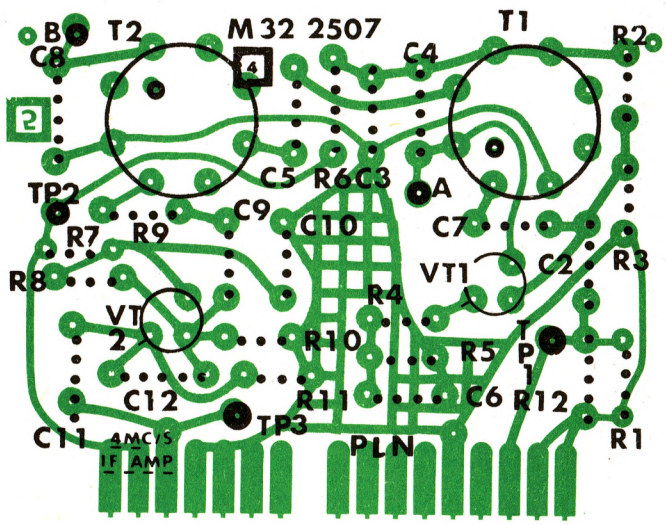
Electrical Description

Figure 4.2

4. The amplifier consists of an amplifier VT1, which contains a pair of band-pass circuits as its collector load, and an emitter follower output stage VT2 which provides a suitable signal source for the frequency changer stage which follows. VT2 also isolates the frequency changer from the band-pass circuits in VT1 collector.

5. The 4 MHz output from the crystal filter is fed to VT1 base via C2. R1 and R12 provide a matching load for the crystal filter. Potential divider R2, R3 provides the base voltage level and with R4 and R5 controls the emitter current of VT1. R4 is un-bypassed and produces negative feedback. The collector load of VT1 is the tuned circuit T1, C4 coupled by C5 to the tuned circuit T2, C8. The two tuned circuits thus form a band-pass pair.

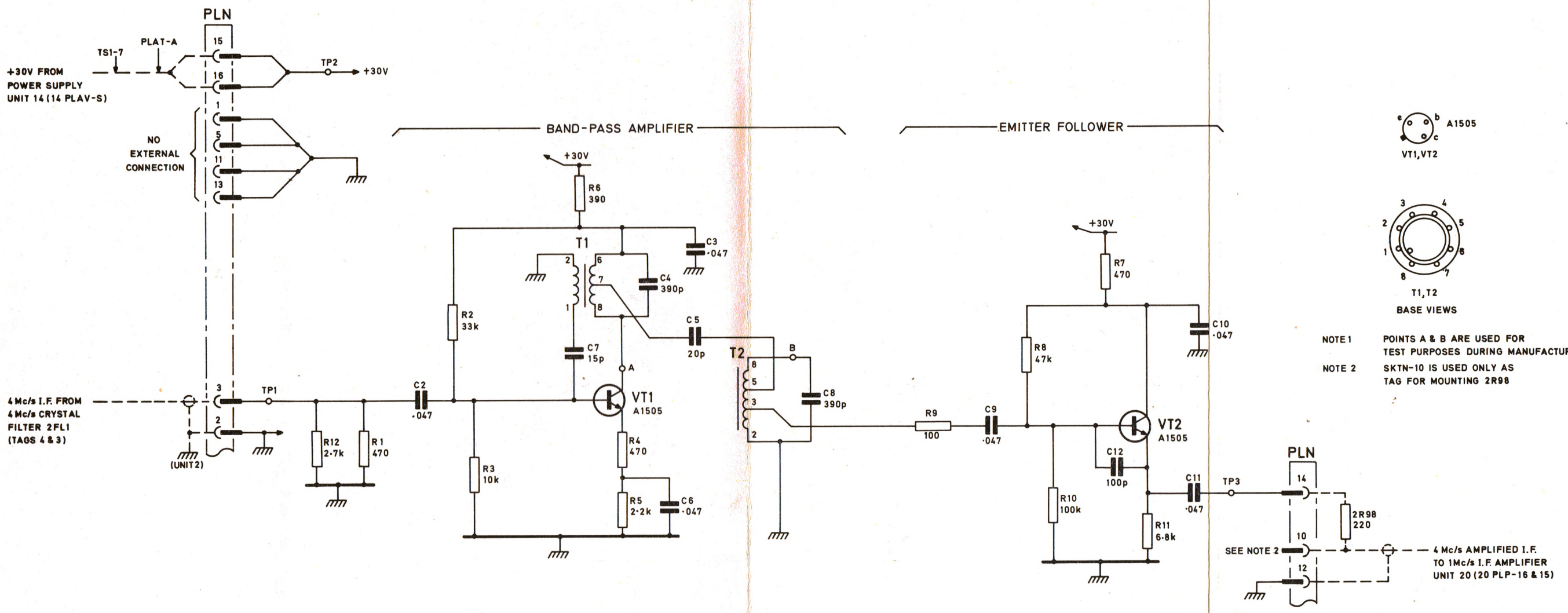
6. The output from VT1 is coupled to the base of emitter follower VT2 by R9 and C9. C12 and R9 counteract any tendency toward high-frequency instability in VT2. The d.c. conditions of VT2 are set in a similar manner to those of VT1. The output of VT2 is fed via C11 to the frequency changer circuit on the 1 MHz I.F. Amplifier.



M32 2507 ISS4 (L)

FIG. 4.1 4MHz I.F. AMPLIFIER COMPONENT LAYOUT

RES	12 1 2 3 6 4 5 9 8 10 7 11
CAP	2 7 4 6 3 5 8 9 12 10 11
MISC	T1 VT1 T2 VT2



MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

4Mc/s I.F. AMPLIFIER 5820-99-521-9418

SUB ASSEMBLY 19 CIRCUIT DIAGRAM

FIG.4·2

CHAPTER 5

1 MHZ I.F. AMPLIFIER 5820-99-521-9416

UNIT 20

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Electrical Description	6 - 9

ILLUSTRATIONS

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1 MHz I.F. Amplifier Functional Diagram	5.1
1 MHz I.F. Amplifier Component Layout	5.2
1 MHz I.F. Amplifier Circuit Diagram	5.3

CHAPTER 5

1 MHZ I.F. AMPLIFIER 5820-99-521-9416

UNIT 20

Introduction

Figure 5.1

1. On ranges 1 to 4 (up to 8 MHz) the First Frequency Changer Unit 21 provides an input of 1 MHz at PLP10.

2. On ranges 5 and 6 (above 8 MHz) the 4 MHz I.F. Amplifier Unit 19 provides 4 MHz at PLP16 which is mixed with 3 MHz, from the 1.1 and 3 MHz Amplifier Unit 23, in frequency changer MR2 to MR5 to produce 1 MHz.

3. When an external VLF adaptor is used it provides an input of 1 MHz at PLP8.

4. One of these sources, determined by the bias condition of diode switches MR6, MR7, MR8, provides the 1 MHz input to the tuned amplifier VT1, VT2, VT3. The output from VT3 is mixed with 1.1 MHz, from the 1.1 and 3 MHz Amplifier Unit 23, in frequency changer MR9 to MR12 to produce an output of 100 kHz at PLP3.

Physical Description

5. Unit 20 is a plug-in printed wiring board 8.2 inches by 3.1 inches. It is in a metal screening box and access is gained by removing the cover. Slotted guides assist location of the board into its socket. Four preset potentiometers, adjusted during initial setting-up, are mounted on the panel. Ten test points are provided on the component side of the board. Points A, B, C and D are used for testing during manufacture.

Electrical Description

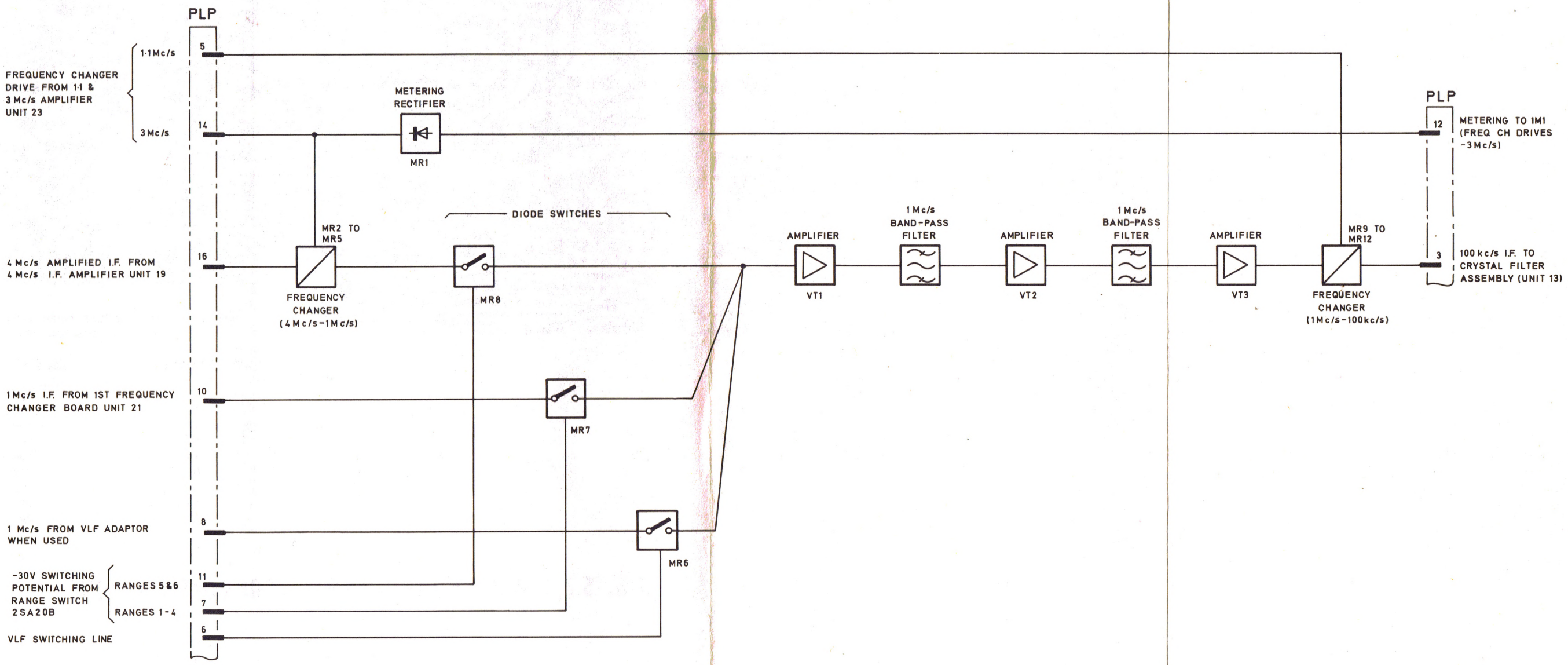
Figure 5.3

6. The 1 MHz signal from the First Frequency Changer at PLP10, 9 passes to VT1 base via C8 and MR7. MR7 is a diode switch that, on ranges 5 and 6, is biased into a non-conducting condition by a positive potential across R8, R9 and R10. In this condition MR7 becomes a high resistance and, in conjunction with R11, constitutes an attenuator network. On ranges 1 to 4 -30 V is applied to PLP7, MR7 conducts via R11, R8 and R9 and allows the 1 MHz signal to pass with negligible attenuation.

7. When an external VLF adapter is used, the 1 MHz input signal is fed to the base of VT1 via C5 and MR6. The action of MR 6 is identical to that of MR7.

8. On ranges 5 and 6 the Receiver is operating in its triple superheterodyne condition. The 4 MHz input at PLP16, 15 is fed to the primary of the pre-tuned transformer T1 which with T2 and MR2 to MR5 comprises a double balanced frequency changer. The 4 MHz input is the low-level and the 3 MHz input the high-level drive. The 3 MHz signal is applied via R3 and R4 to the secondary of T1, and via RV1 and RV2 to the primary of T2. RV1 and RV2 are used to balance out the amount of 3 MHz appearing in the output of the frequency changer. MR2, MR3 and MR4, MR5 conduct on alternate half-cycles of the drive signal and provide the frequency changing action. C13 tunes the secondary of T2 to 1 MHz. The 3 MHz drive level is rectified by MR1, smoothed by C4, R2 and monitored by the front panel METERING Switch and meter. The output of the frequency changer is fed via switching diode MR8 to the base of VT1. The action of MR8 is identical to that of MR7 but it is switched into the conducting condition on ranges 5 and 6.

9. The 1 MHz Amplifier consists of VT1 and VT2 in cascade, followed by emitter follower VT3. The band-pass circuits complement each other to give a reasonably flat passband response and adequate attenuation at second channel frequency (1.2 MHz). The base reference voltage of VT1 is set by the potential divider R15, R16 and with R19 and R20 controls the emitter current. R19 provides a.c. negative feedback. The action of VT2 is the same as that of VT1. VT1 is neutralised by the secondary of T3 and C17. The output from the secondary of T5 is coupled via C32 to VT3 the output of which is coupled via C35 to the primary of T7. This is the low-level input to the final frequency changer which is similar in action to the 4 MHz to 1 MHz frequency changer. The high-level input is 1.1 MHz. The output signal of 100 kHz is taken from the secondary of T6.

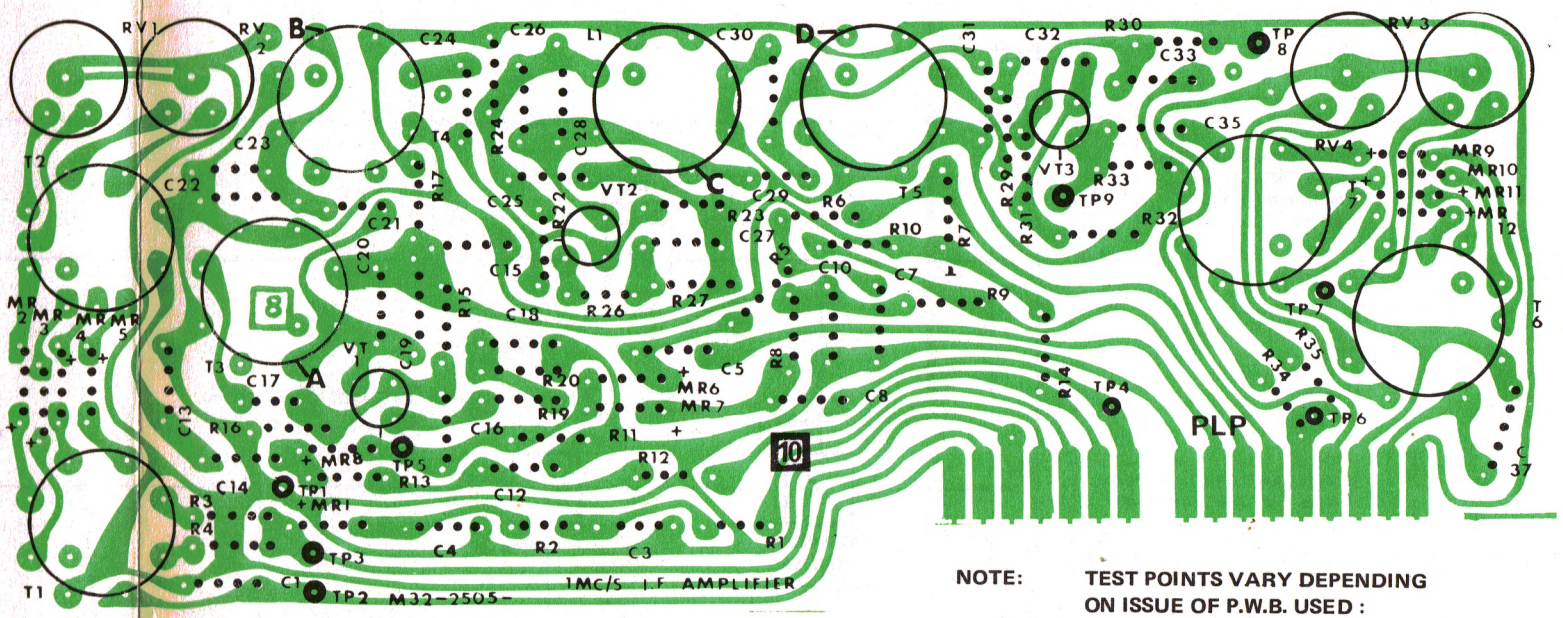


1Mc/s I.F. AMPLIFIER
SUB ASSEMBLY 20

5820-99-521-9416
BLOCK DIAGRAM

FIG. 5·1

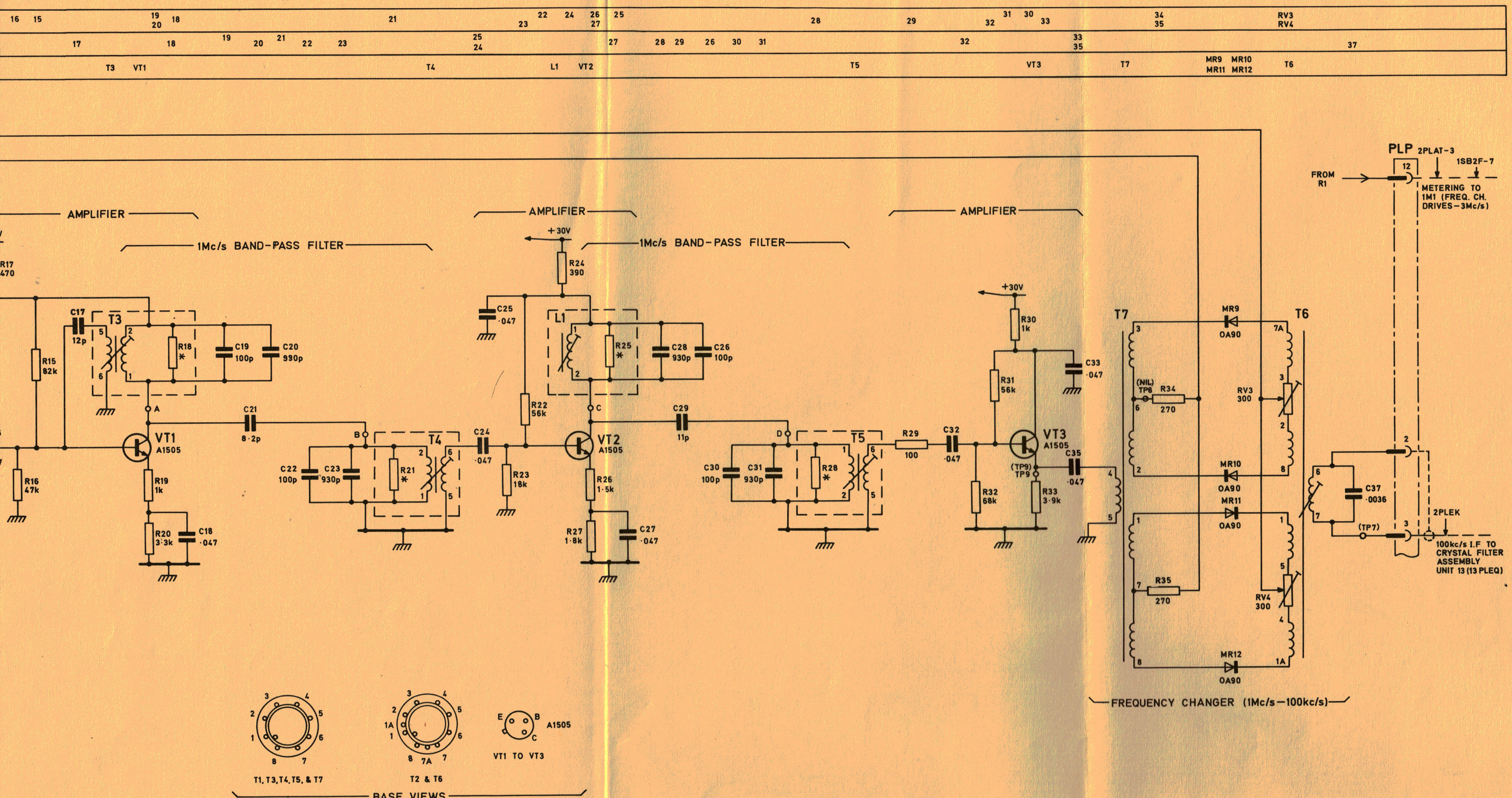
M32 2505 L ISS 10



NOTE: TEST POINTS VARY DEPENDING ON ISSUE OF P.W.B. USED :

UP TO ISSUE 8	ISSUE 9 UPWARDS
NIL	TP1
TP2	TP2
TP7	TP3
TP5	TP4
NIL	TP5
NIL	TP6
NIL	TP7
TP10	TP8
TP9	TP9

FIG. 5.2 1 MHz I.F. AMPLIFIER COMPONENT LAYOUT



NOTES: RESISTORS MARKED THUS * SELECTED ON COIL TESTS

LETTERED POINTS ARE USED FOR TEST PURPOSES DURING MANUFACTURE

ALL EARTH POINTS ARE COMMON

TEST POINTS SHOWN WITHOUT BRACKETS ARE ON THE P.W. Bs UP TO ISSUE 8 INCLUSIVE.

TEST POINTS SHOWN IN BRACKETS ARE ON THE P.W. Bs AT ISSUE 9 AND ABOVE.

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

1Mc/s I.F. AMPLIFIER 5820-99-521-9416

SUB-ASSEMBLY 20 CIRCUIT DIAGRAM

FIG.5·3

| | | |

CHAPTER 6

F.O.S.U. WIDE-BAND AMPLIFIER

M32-5269-01

UNIT 24

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Introduction	1
Physical Description	2
Electrical Description	3, 4

ILLUSTRATIONS

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F.O.S.U. Wide-band Amplifier Component Layout	6.1
F.O.S.U. Wide-band Amplifier Circuit Diagram	6.2

CHAPTER 6

F.O.S.U. WIDE-BAND AMPLIFIER

M32-5269-01

UNIT 24

Introduction

1. The Wide-band Amplifier amplifies the output of the Frequency Offset Unit, unit 3 to provide a suitable signal to the First Oscillator tuned filter. It has a gain of 26 dB with an input impedance of 150 ohms and an output impedance of 75 ohms. The main output is 200 mV over the frequency range 1 to 32 MHz. An additional output of about 20 mV is available for use with a VLF adaptor or to supply a second Receiver for diversity operation.

Physical Description

Figure 6.1

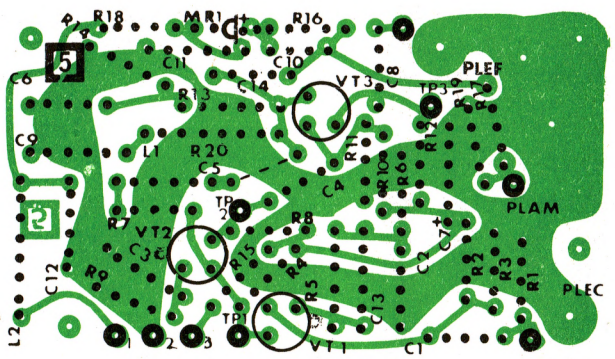
2. Unit 24 is a printed wiring board 3.6 inches by 2.5 inches. It is secured by four screws in a metal screening box that is secured to the Tuning Unit, Receiver by four screws. Signal connections are made by three coaxial plugs but metering and supply connections are made by three soldered terminal posts. Three test points are provided on the component side.

Electrical Description

Figure 6.2

3. Three stages of amplification employ frequency-selective feedback which stabilises the gain. The output stage VT3 operates with a current such that the stage will not limit in the event of the terminating impedance becoming low.

4. Facilities are provided for metering the output level. MR1, a back-biased diode, allows a portion of the output to be rectified and applied to the meter on the front panel, when the METERING switch is set to position 10 (1st OSC FREQ CH. DRIVES).



M32-5269L ISS5

FIG. 6.1 F.O.S.U. WIDEBAND AMPLIFIER COMPONENT LAYOUT

| | | |

CHAPTER 7

100 KHZ A.F. OSCILLATOR 5820-99-521-9420

UNIT 22

CONTENTS LIST

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Introduction	1, 2
Physical Description	3, 4
ELECTRICAL DESCRIPTION	5 - 14
100 kHz Buffer Amplifier	5
Diode Switches	6, 7
100 kHz Crystal Controlled Oscillator	8 - 12
Frequency Changer	13, 14

ILLUSTRATIONS

	Figure No
100 kHz A.F. Oscillator Block Diagram	7.1
100 kHz A.F. Oscillator Component Layout	7.2
100 kHz A.F. Oscillator Circuit Diagram	7.3

CHAPTER 7

100 KHZ A.F. OSCILLATOR 5820-99-521-9420

UNIT 22

Introduction

Figure 7.1

1. The 100 kHz Oscillator provides a low level output of 1.1 MHz by mixing a 1 MHz 200 mV signal from the 1 MHz Limiter unit 25 with a 100 kHz 500 mV signal. The mixer is a switching-type frequency changer.

2. When the receiver FINE TUNING control is set to 0 the 100 kHz input is from the Synthesiser. When the control is set to any other position the 100 kHz input is from a crystal controlled oscillator on the board. The nominal 1.1 MHz output can then be 'pulled' in 10 Hz steps by the FINE TUNING CONTROL.

Physical Description

3. Unit 22 is a plug-in printed wiring board 6.4 inches by 2.5 inches. It is in a metal screening box at the front of unit 2 and access is gained by removing the cover. Slotted guides assist location of the board and dowels on the printed wiring side prevent it being inserted in the wrong position.

4. A preset potentiometer, adjusted during initial setting-up, is mounted on the board. Ten test points are provided on the component side.

ELECTRICAL DESCRIPTION

Figure 7.3

100 kHz Buffer Amplifier

5. The 100 kHz input from the Frequency Synthesiser at PLR8, 9 passes via C1 to the base of common emitter amplifier VT1. The output is directly coupled to emitter follower VT2. R2, R3 set the base reference voltage and, with R4, R5, the emitter current of VT1. R4 is un-bypassed to a.c. thereby providing high negative feedback. The current of VT2 is set by R7 and the supplies for VT1, VT2 are filtered by R6, C3.

Diode Switches

6. The output of VT2 passes to PLR4 via C4 and diode switch MR1 which is forward biased by -30 V from PLR7 when the FINE TUNING control is set to 0. The d.c. return path for MR1 is via R31.

7. When the FINE TUNING control is at any position other than 0 diode MR1 is reverse biased by +30 V via R8 and -30 V is applied to PLR5 to activate the 100 kHz crystal oscillator circuit and to forward bias MR5.

100 kHz Crystal Controlled Oscillator

8. VT3, VT4, VT5 and crystal XL1 form the oscillator. At approximately 100 kHz the crystal resistance is low and the phase relationship favours oscillation provided the amplifier has sufficient gain. At other frequencies the crystal has a high series resistance and, with VT4 input resistance, produces a high circuit loss which with unsuitable phase conditions prevents oscillations. To obtain slight variations in frequency a varactor diode MR4 is connected in series with the crystal and controlled by a variable supply from 0 V to 70 V.

9. The base reference voltage of VT3 is set by R11 and R12 and with R15 and R16 controls the emitter current. The un-bypassed resistor R15 provides high negative feedback. The +30 V supply to VT3 and VT4 is decoupled by R17, C6 and R19, C15. The d.c. conditions for VT4 are set in the same manner as those for VT3.

10. Overall feedback to maintain oscillations is provided from VT4 collector via C9 and R13 to VT3 base. Once oscillations have commenced their amplitude is clamped by MR2, MR3.

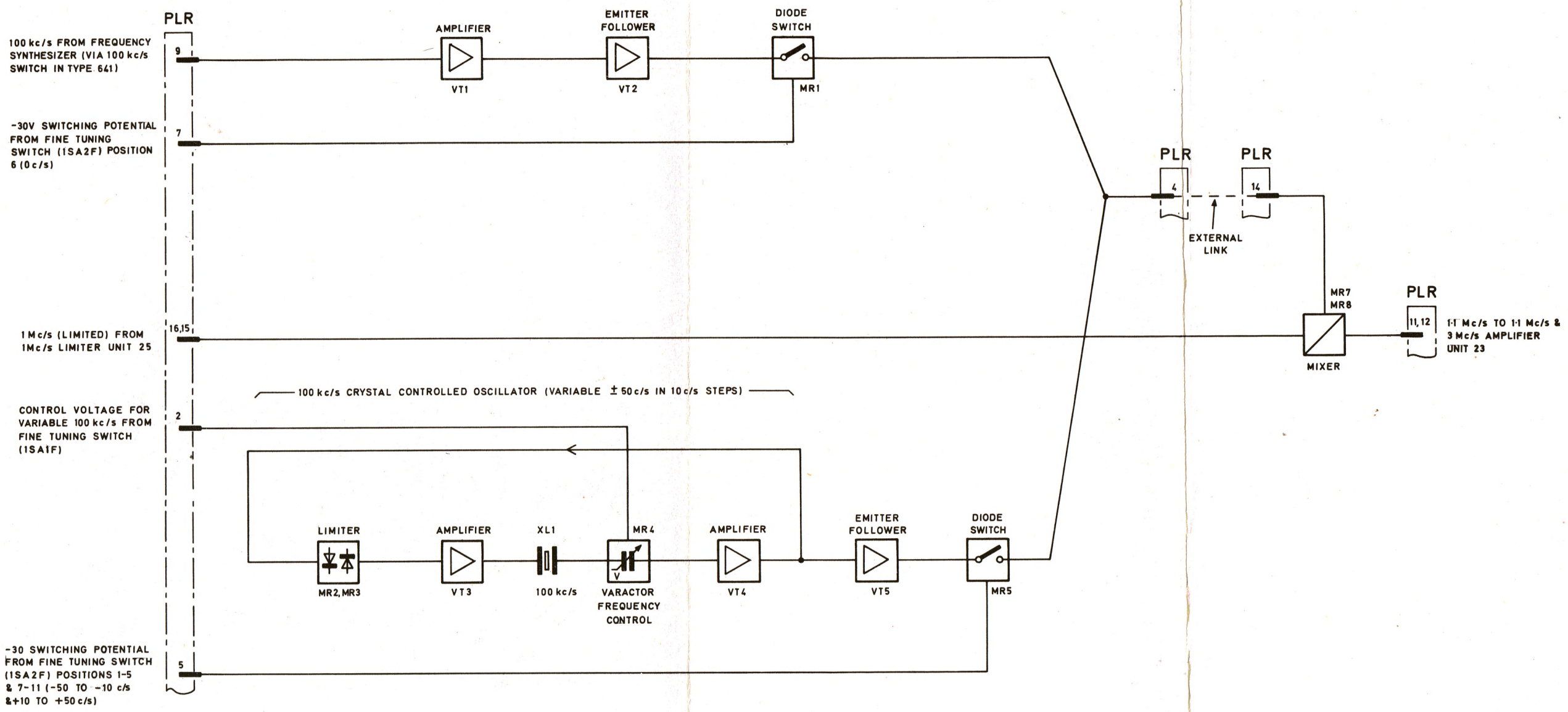
11. Varactor diode MR4 is controlled by a positive potential applied to the cathode via the decoupling network C12, R21, C10, R20. R18 provides a return path for MR4 leakage current. The positive potential is derived from a fixed potential divider network switched by the FINE TUNING control. 1RV3, 1RV4 are provided for adjusting the 100 kHz centre frequency and the high-frequency end of the range.

12. VT4 output is directly coupled to emitter follower VT5 which provides, via C16 and diode switch MR5, the alternative output at PLR4. MR5 is switched on at the same time as the oscillator ie when -30 V is applied to PLR5 by the FINE TUNING control.

Frequency Changer

13. The 100 kHz output from either source is linked back to PLR14 and via R34, which sets the drive source impedance, to the centre-tapped secondary of the 1 MHz input transformer T1. The 1 MHz input is via PLR15, 16 to T1 primary. The frequency changer is single balanced with T1 untuned.

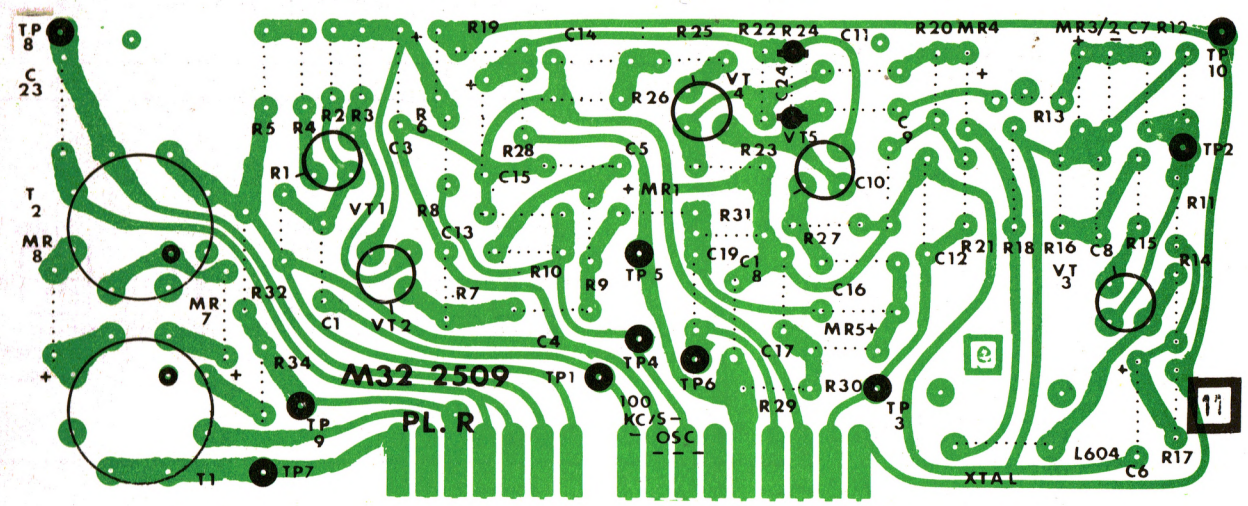
14. Output transformer T2 is tuned to 1.1 MHz by C23. R23 provides a d.c. return path for frequency changer diodes MR7, MR8. The 1.1 MHz constituent is peaked by the trimmer of T2 and the output from the secondary, at a level of 400 to 600 mV, is taken to the 1.1 MHz and 3 MHz Amplifier Board, unit 23, from PLR11, 12.



100kc/s A.F. OSCILLATOR 5820-99-521-9420

SUB-ASSEMBLY 22 BLOCK DIAGRAM

FIG.7·1

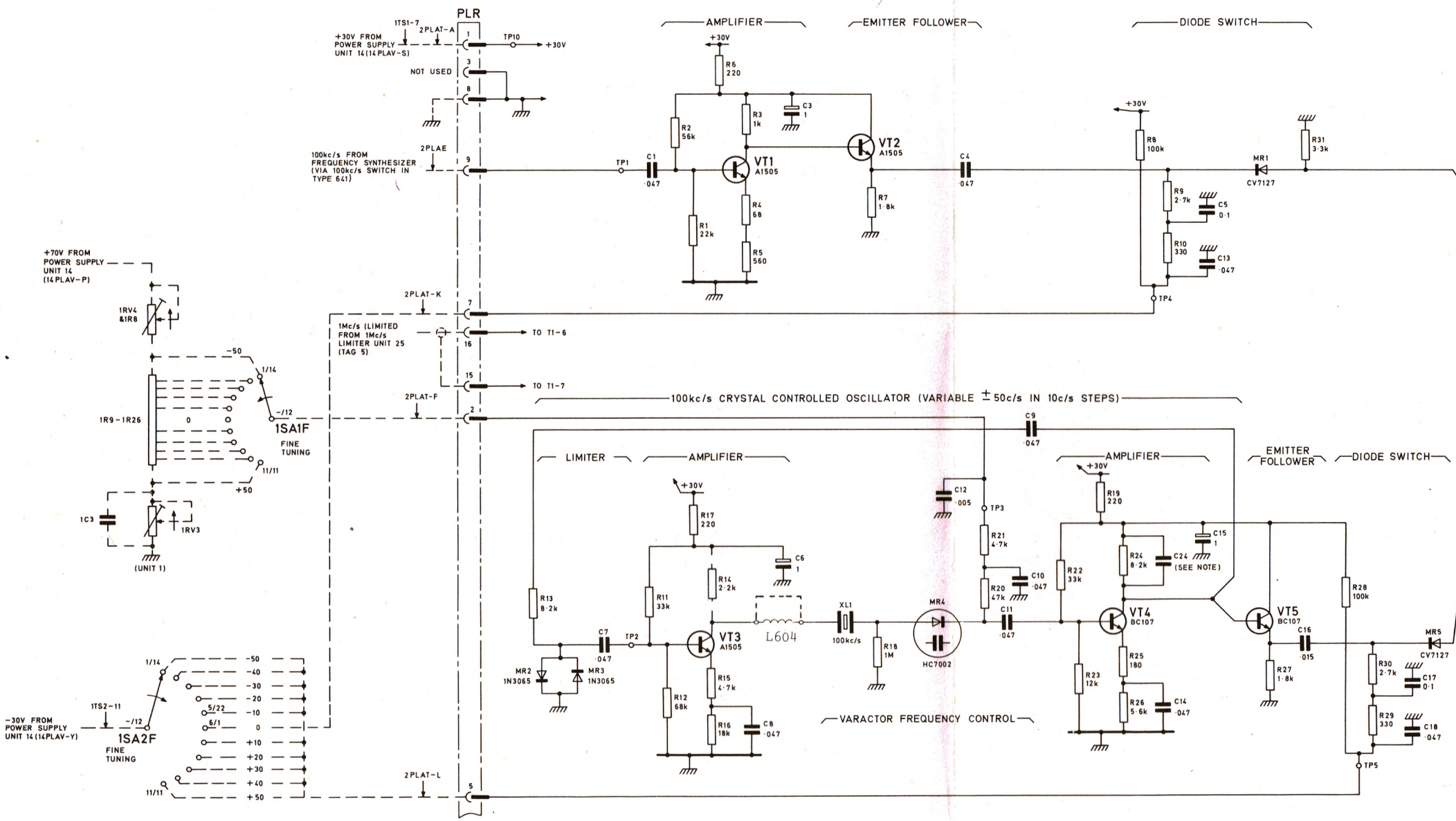


M32-2509 ISS11 (L)

FIG. 7.2 100 kHz A.F. OSCILLATOR COMPONENT LAYOUT

BR 4147 (5) A
Amdt. 5, 2.82

RES.	13 11 2 1 12 17 14 6 15 16 3 4 5 7 18 21 20 22 19 24 8 9 10 23 25 26 27 31 28 30 29 34 32
CAP.	7 1 8 6 3 12 4 11 10 9 24 14 5 15 13 16 17 18 19 23
MISC.	MR2 MR3 VT3 VT1 L604 XL1 VT2 MR4 VT4 MR1 VT5 MR5 T1 T2



NOTE: CAPACITOR C24 IS SELECTED ON TEST (IN RANGE 18p-47p)

MOD RECORD

1	2	3	4	5	6	
7	8	9	10	11	12	

100kc/s A.F. OSCILLATOR 5820-99-521-9420

SUB-ASSEMBLY 22 CIRCUIT DIAGRAM

FIG. 7·3

CHAPTER 8

1.1 MHZ AND 3 MHZ AMPLIFIER BOARD

5820-99-521-9419

UNIT 23

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ILLUSTRATIONS

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1.1 MHz and 3 MHz Amplifier Component Layout	8.2
1.1 MHz and 3 MHz Amplifier Circuit Diagram	8.3

CHAPTER 8

1.1 MHZ AND 3 MHZ AMPLIFIER BOARD

5820-99-521-9419

UNIT 23

Introduction

Figure 8.1

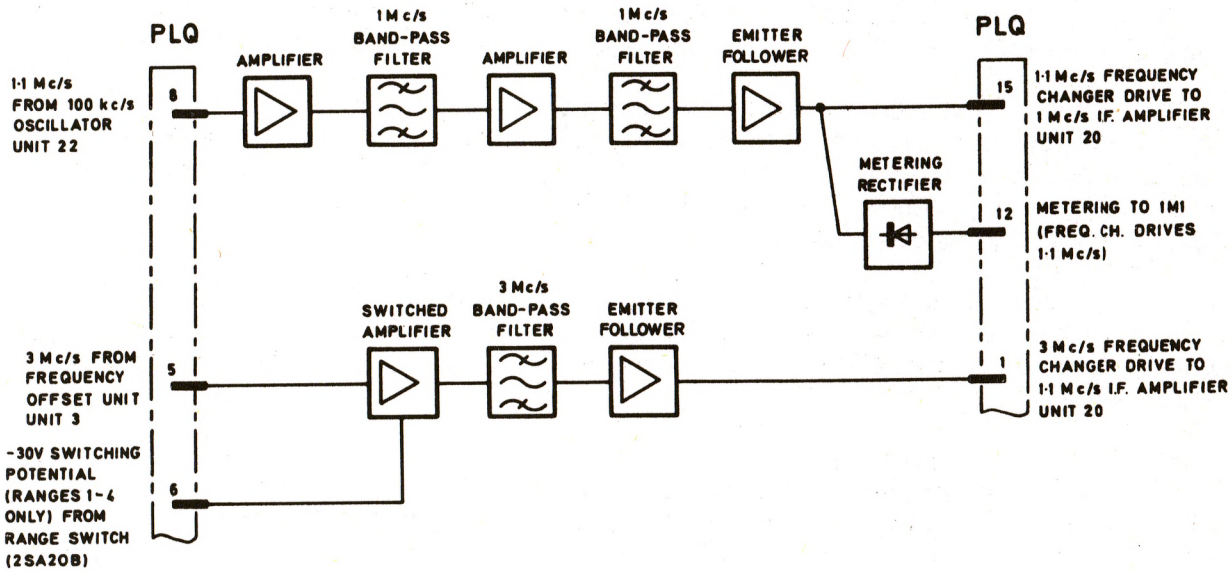


FIG.8·1 1 Mc/s & 3Mc/s AMPLIFIER 5820-99-521-9419 SUB-ASSEMBLY 23 BLOCK DIAGRAM

1. Separate 1.1 MHz and 3 MHz amplifier and filter circuits provide outputs for the 1 MHz I.F. Amplifier Unit 20.

2. The 1.1 MHz circuit comprises two tuned amplifier stages and an emitter follower. It amplifies the low-level input from the 100 kHz Oscillator Unit 22 to a level suitable for the final frequency changer. A metering output is provided at PLQ12.

3. The 3 MHz amplifier, comprising one tuned amplifier and an emitter follower, amplifies the low-level signal from the F.O.S.U. Unit 3 to a level suitable for the second frequency changer. It is inhibited on ranges 1 to 4 by -30 V from 2SA20B.

Physical Description

4. Unit 23 is a plug-in printed wiring board 6.4 inches by 2.5 inches. It is in a metal screening box and access is gained by removing the cover. Slotted guides assist location of the board and dowels on the printed-wiring side prevent it being inserted in the wrong position.

5. Seven test points are provided on the component side. Points A, B, C, D are used for testing during manufacture.

Electrical Description

Figure 8.3

6. The 1.1 MHz input signal is applied to VT1 base via C1. Potential divider R1, R2 sets the base reference voltage and with R4 and R5, controls the emitter current.

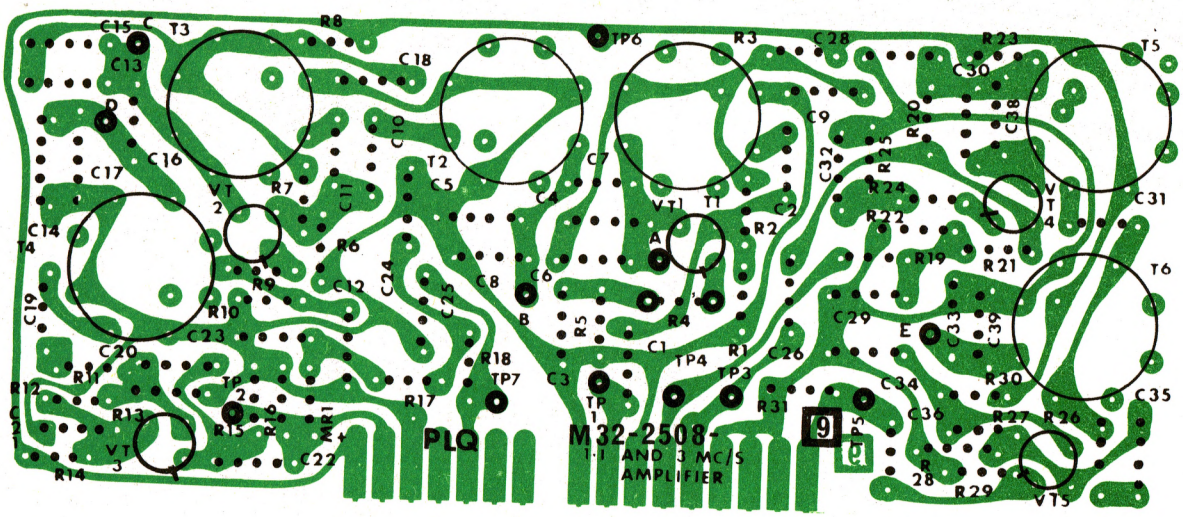
7. The collector load is formed by the pair of tuned band-pass circuits T1, C4, C6 and T2, C5, C8 coupled by C7. Neutralisation of VT1 is achieved by the secondary winding of T1 and C2. The output of VT1 is coupled to VT2 base via the secondary winding of T2 and C10. The +30 V supply is filtered by R3 and C9.

8. VT2 is identical to VT1. Its output is coupled to the base of emitter follower VT3 via the secondary winding of T4 and C19. The d.c. conditions of VT3 are set in a similar way to those of VT1 and VT2. At high frequencies unwanted oscillations are reduced by R11 and C20. The output from VT3 emitter is the input to the final frequency changer in Unit 20.

9. A metering output is rectified by diode MR1 and filtered by C23, R17, C24, R18, C25. This provides an indication of the 1.1 MHz signal on the front panel meter when the METERING switch is set to position 12 (1.1 MHz FREQ CH. DRIVES).

10. The 3 MHz amplifier has one stage of amplification, which operates in the same way as the 1.1 MHz amplifiers. The 3 MHz input from the Frequency Offset Unit is coupled to VT4 base by C26. The tuned band-pass circuits T5, C30, C38, and T6, C33, C39 coupled by C31 are tuned to 3 MHz. The output is taken from a tapping point on T6 via R26 and C35 to the base of the emitter follower VT5. The output from VT5, via C36, is the input to the second frequency changer in Unit 20.

11. The 3 MHz amplifier is used only when the range switch is on position 5 or 6. On ranges 1 to 4 -30 V d.c. is applied via R19, R22, C29 to VT4 base, thus biasing it off.



M32 2508 L 1559

FIG. 8.2 1.1 MHz AND 3MHz AMPLIFIER COMPONENT LAYOUT

| | | |

CHAPTER 9

1 MHZ LIMITER BOARD M32-3766-01

UNIT 25

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	Paragraphs
Introduction	1 - 3
Physical Description	4, 5
Electrical Description	6 - 9

ILLUSTRATIONS

	Figure No
1 MHz Limiter Block Diagram	9.1
1 MHz Limiter Component Layout	9.2
1 MHz Limiter Circuit Diagram	9.3

CHAPTER 9

1 MHZ LIMITER BOARD M32-3766-01

UNIT 25

Introduction

Figure 9.1

1. The 1 MHz Limiter accepts a variable level of input from the external Frequency Standard and provides three outputs of relatively constant level.

2. The 1 MHz input is applied to two circuits each comprising a buffer amplifier, a diode limiter and an output transformer. Separate amplifiers are used to isolate the 1 MHz lines to the 100 kHz Oscillator and the Frequency Offset Unit. The limiting action will reduce a variation of, say, 10 dB in input level to one of less than 3 dB in output level.

3. When the front panel METERING switch is set to position 19, diode switch MR7 is switched on by -30 V to provide the third output. This is a 1 MHz test signal and the d.c. switching potential for 21MR11 in the First Frequency Changer.

Physical Description

4. Unit 25 is a printed wiring board 3.2 inches by 1.4 inch. It is held by two screws in a metal screening box and access is gained by removing the cover. Connections are made by two coaxial plugs, one miniature coaxial plug and soldered wire.

5. The box is hinged on the right-hand side, and there is a hole in the cover so that a captive screw can be released, to allow access to components underneath.

Electrical Description

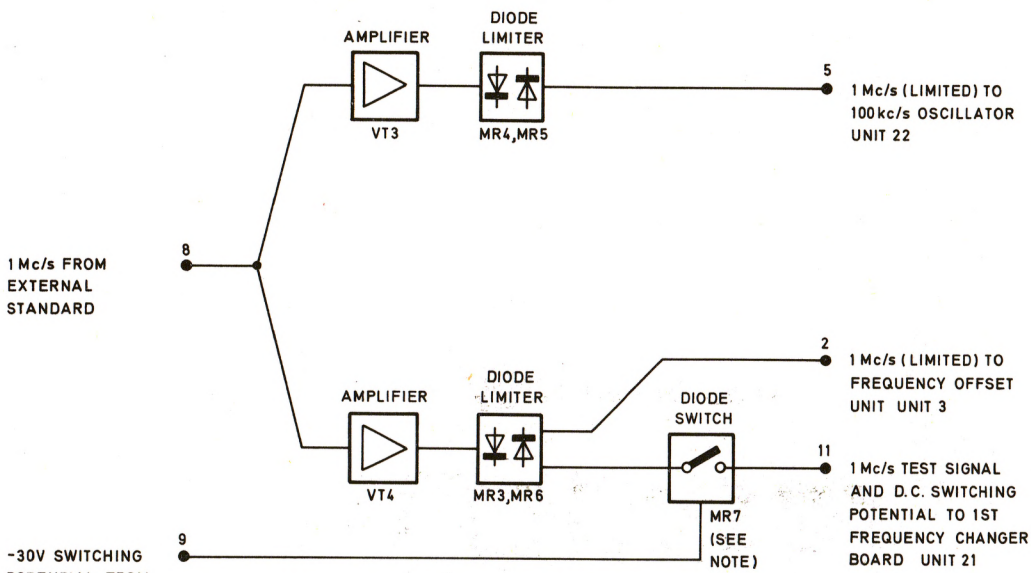
Figure 9.3

6. The 1 MHz input from the Frequency Standard is fed to the base of buffer amplifiers VT3 and VT4 via C106.

7. Under start and low-level conditions the load on VT3 comprises TR1 and the reflected impedance. As the voltage of the output signal rises above the threshold level of the silicon diodes MR4 and MR5 (approximately 400 mV), the load becomes sufficient to clamp the output signal, each diode conducting on alternate half cycles. TR1 isolates the 1 MHz source from its limited 1 MHz output which is applied to the 100 kHz Oscillator, Unit 22.

8. The action of VT4 is identical to that of VT3. TR2 has two secondary windings, both step down in ratio. One winding supplies the Frequency Offset Unit, unit 3, whilst the other provides the 1 MHz test supply to Unit 21. R89, R90 and R91 set the level of the 1 MHz test supply.

9. MR7 is switched on by -30 V d.c. via R92, decoupled by C107, when the METERING switch is set to position 19. The 1 MHz test signal is at microvolt level and MR7 remains non-conductive until the threshold level of 400 mV is reached.



NOTE. THE SWITCHING CURRENT WHICH CAUSES MR7 TO CONDUCT ALSO PASSES VIA TAG 11 IN ORDER TO ACTIVATE A SIMILAR DIODE SWITCH IN UNIT 21

1Mc/s LIMITER **M32-3766-01**
SUB-ASSEMBLY 25 BLOCK DIAGRAM

FIG. 9·1

M32 3766 ISS 7 L

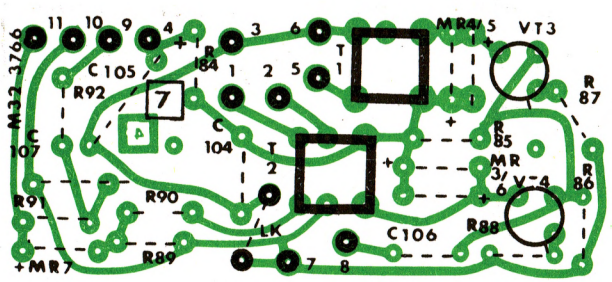


FIG. 9.2 1 MHz LIMITER BOARD COMPONENT LAYOUT

| | | |

CHAPTER 10

FREQUENCY OFFSET UNIT 5820-99-519-7027

UNIT 3

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CHAPTER 10

FREQUENCY OFFSET UNIT 5820-99-519-7027

UNIT 3

Introduction

1. To produce the local oscillator frequency in the Receiver the frequency indicated on the Synthesiser must be offset by the intermediate frequency, which is 4 MHz or 1 MHz depending on the range in use.

2. If the offset was applied directly to the normal Synthesiser output at the indicated frequency there would be a relatively strong signal in the Receiver at the same frequency as the received signal. This would cause a serious spurious response problem.

3. To avoid this the normal indicated frequency output from the Synthesiser is inhibited and the three signals which would have been combined to form it are mixed in the Frequency Offset Unit where the necessary offset is applied during the mixing process.

Physical Description

4. Unit 3 is a printed wiring board 17 inches by 5 inches. It is in a metal screening box formed by two covers, one on each side of the board, which are screwed to hexagonal pillars on the component side of the board. The unit is secured to the chassis by three screws.

5. Connections are made by three MUSA-type coaxial plugs on the board, four sub-miniature coaxial sockets on flying leads and a 14-way plug. Eight preset potentiometers, adjusted during the initial setting-up, are mounted on the board. Test points are provided on the component side.

ELECTRICAL DESCRIPTION

Principle of Operation

Figure 10.1

6. The signal inputs to the Frequency Offset Unit are the major constituent signals in the Frequency Multiplier (MHz) in the Frequency Synthesiser, and the 1 MHz signal from the Frequency Standard.

7. A 3 MHz signal and a 4 MHz signal are produced by applying the 1 MHz input signal from the Frequency Standard to harmonic generators. The 4 MHz so produced and the 37.5 MHz input signal, is applied to the 3rd Mixer thereby producing a frequency of 33.5 MHz. This signal is then applied, together with the 2-3 MHz input signal, to the 1st Mixer which produces a frequency between 35.5 and 36.5 MHz. On ranges 5 and 6, when the required i.f. is 4 MHz, this 35.5-36.5 MHz signal is mixed with the LC oscillator signal of 40.5 MHz - 67.5 MHz in the 4th Mixer. The resultant output, between 12 and 32 MHz, provides the first oscillator frequency on ranges 5 and 6.

8. On ranges 1-4, when the required i.f. is 1 MHz an additional frequency changer is incorporated. The 35.5-36.5 MHz signal, prior to its application to the 4th mixer, is mixed with the 3 MHz harmonic of the Standard 1 MHz signal in the 2nd mixer. Thus, on these ranges 38.5-39.5 MHz is mixed with the LC oscillator signal, providing an output from the 4th mixer of 1-9 MHz.

9. The change from one condition to the other with change of range is accomplished by diode switches. Switching lines from the Ledex-controlled range switch control the bias conditions of the diode switches.

Range Controlled Diode Switches — Figures 10.3, 10.2

10. Two pairs of diode switches gate the signal path from the 35.5-36.5 MHz filter, via the 2nd mixer for 1 MHz i.f. or direct for 4 MHz i.f., to the 4th mixer. They can be considered as a double-pole change-over switch and they are controlled by the Range switch in Unit 2.

11. The operation of each pair of switches is identical and the action of one pair to change-over from one signal path to the other is shown in Figure 10.2. MR15, MR17 in series and MR21, MR18 in series gate the signal path. They are governed by MR14, MR16 and MR22, MR19 respectively, which form shunting paths for the d.c. current.

12. When the range switch selects a range from 1 to 4 the d.c. level at junction R41, L47 is 0 V. MR22, MR19 are forward biased, through their respective resistance chains, to reverse bias MR21, MR18 so that the signal path for 4 MHz is closed. At the same time the d.c. level at junction R32, L46 is +30 V so that MR14, MR16 are reverse biased. This allows MR15, MR17 to be forward biased by the d.c. potential produced from +30 V via R33, R35 respectively, L25, R36 to chassis. The signal path for 1 MHz i.f. is then gated open by MR15, MR17.

13. When the range switch selects range 5 or 6 the d.c. level at junction R32, L46 is 0 V. MR14, MR16 are forward biased, through their respective resistance chains, to reverse bias MR15, MR17 so that the signal path for 1 MHz i.f. is closed. At the same time the d.c. level at junction R41, L47 is +30 V so that MR22, MR19 are reverse biased. This allows MR21, MR18 to be forward biased by the d.c. potential produced from +30 V via R39, R37 respectively, L25, R36 to chassis. The signal path for 4 MHz i.f. is then gated open by MR15, MR17.

Signal Paths and Mixing — Figures 10.3, 10.5A, B

14. The 1 MHz Standard input at SKTED is applied to the bases of harmonic generators VT7, VT8. The bias arrangements in each of these stages produces a distorted output rich in harmonics.

15. The output of VT7 is tuned to select the 4 MHz harmonic of the 1 MHz input and is applied via C78 to the base of VT4, the 3rd mixer. Here it is heterodyned with the incoming 37.5 MHz signal at PLAK, from the Synthesiser, to produce an output of 33.5 MHz. Provision is made to meter the 37.5 MHz incoming signal at PLAW, E via MR20, C44, R30. Both input signals to VT4 are at a relatively low level to keep spurious signal production at a minimum.

16. The 33.5 MHz output from VT4 is applied to a two-stage tuned amplifier VT5, VT6 which raises the signal level to provide a suitable switching signal to the 1st mixer.

17. The 33.5 MHz output from VT6 serves as the high level switching signal to the 1st mixer MR1-4. The 2-3 MHz incoming signal at PLAH, from the Synthesiser, is the low-level modulating signal. The resultant output of 35.5 - 36.5 MHz is applied to tuned amplifier VT1, via a band-pass filter formed by the triple coupled circuit L2, L3, L4. Provision is made to meter the 2-3 MHz incoming signal at PLAW(J) via MR10 rectifier circuit.

18. After further filtering by L5, L6, L7, the signal is applied to the diode switching circuit. See Paragraphs 10 to 13.

19. On ranges 5 and 6 the 35.5 - 36.5 MHz signal is routed, via the diode switching circuits, to the 4th mixer. On ranges 1-4 the signal is routed by diode switching to a two-stage amplifier VT14, VT2 where its level is raised to form the switching signal to the 2nd mixer MR5-8.

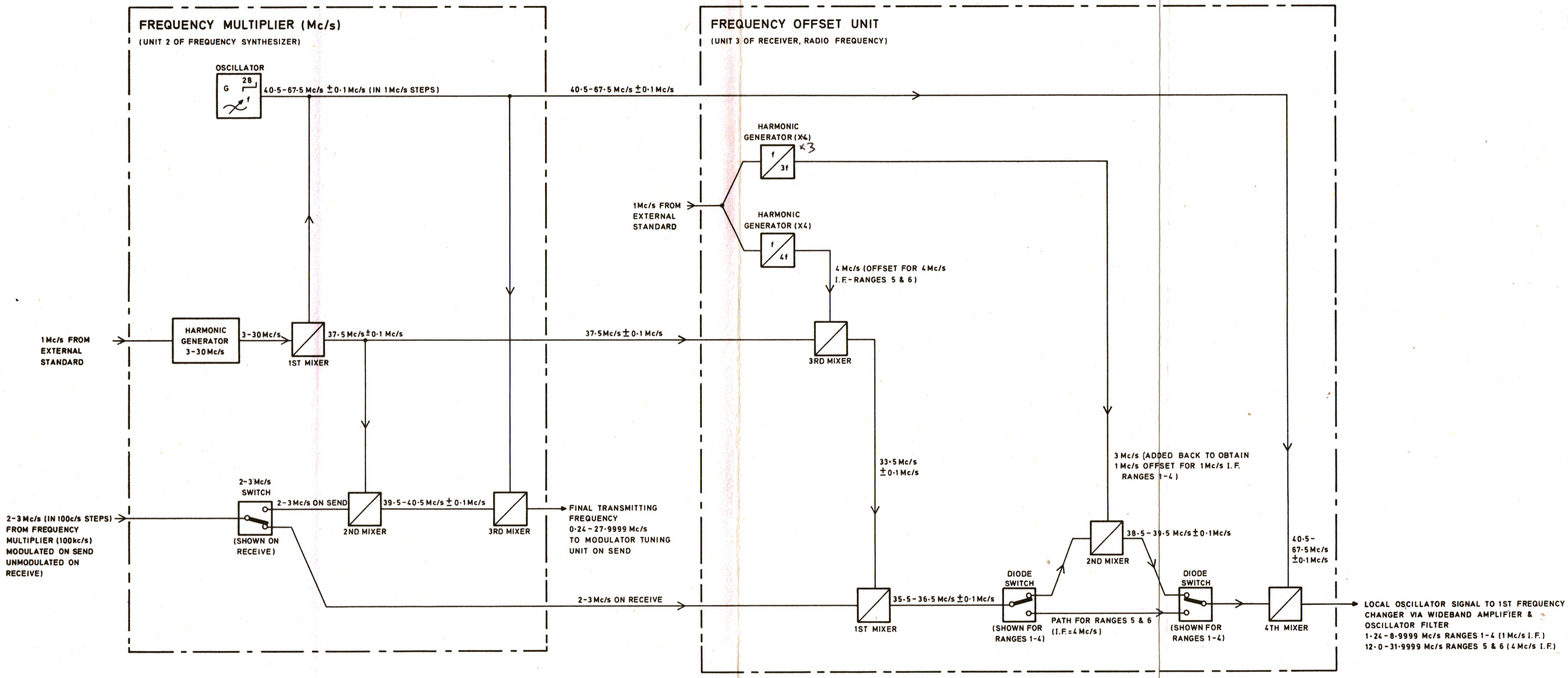
20. The output of VT8 is tuned to select the 3 MHz harmonic of the 1 MHz input from the Frequency Standard. This 3 MHz signal is applied to the primary of transformer L33. One secondary of L33 provides a 3 MHz signal to the 1.1 MHz and 3 MHz Amplifier Unit 23 via SKTEE. Another secondary of L33 applies a low-level 3 MHz signal to the 2nd mixer via RV10.

21. The resultant output from the 2nd mixer of 38.5 MHz to 39.5 MHz is applied to tuned amplifier VT3 and then, via diode switches, to the 4th mixer.

22. Thus, depending on the range in use, the low-level input to the 4th mixer is 35.5 MHz to 36.5 MHz or 38.5 MHz to 39.5 MHz. The high-level switching signal to the 4th Mixer is the Frequency Synthesiser LC oscillator 40.5 MHz to 67.5 MHz signal, suitably amplified by VT9, VT11.

23. The resultant output from the 4th Mixer, either 1.24 MHz to 8.9999 MHz on ranges 1-4 or 12 MHz to 31.9999 MHz on ranges 5 and 6, is the output from the unit which is taken from SKTEC to the F.O.S.U. Wide-band Amplifier Unit 24.

24. Outputs at 3 MHz and 4 MHz are fed to the 1.1 MHz and 3 MHz Amplifier, Unit 23 and to the First Frequency Changer, Unit 21 via SKTEE and SKTET respectively.

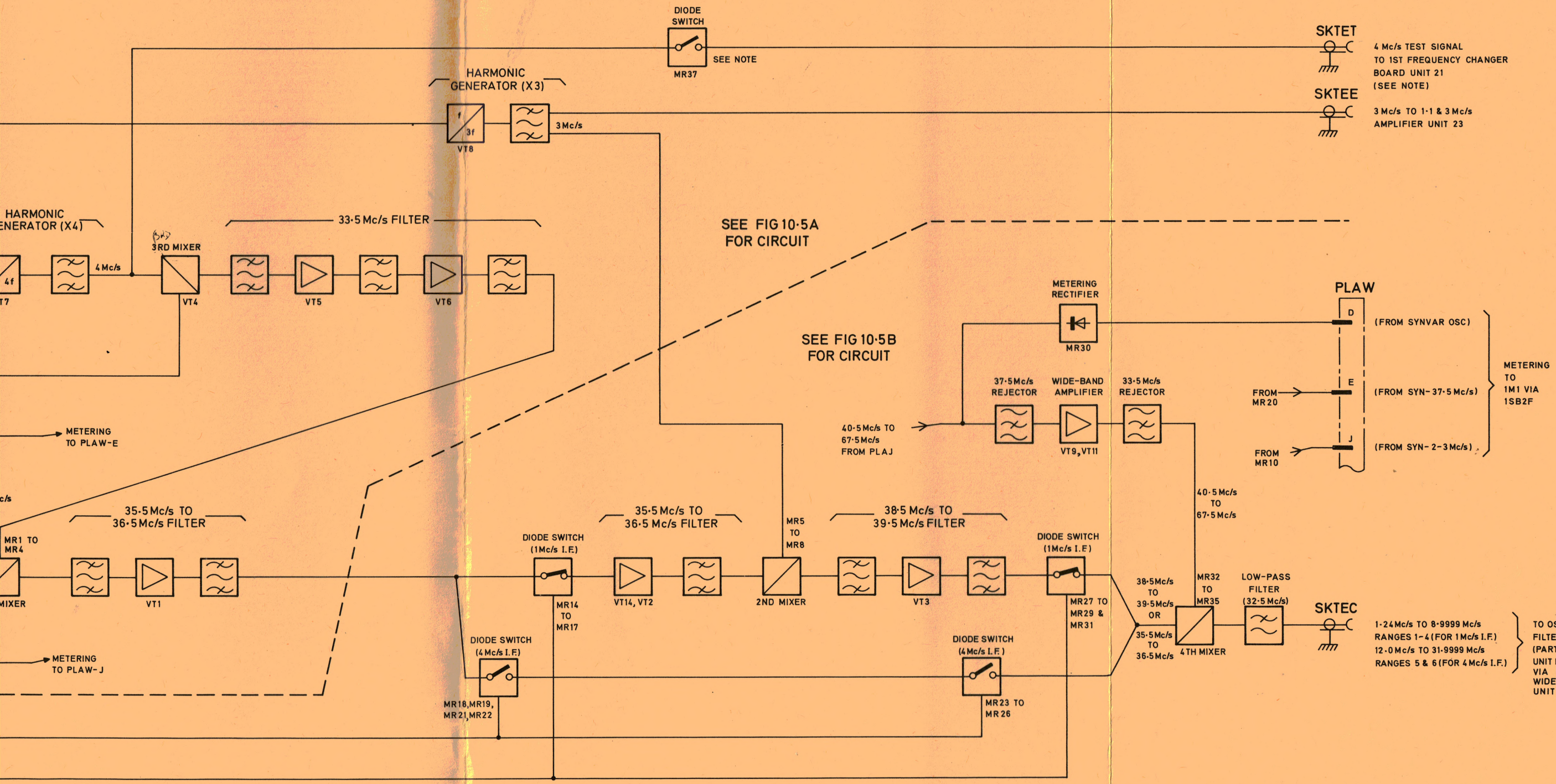


NOTES.
1. THE FREQUENCY ERROR OF THE 40·5-67·5 Mc/s OSCILLATOR IS SELF-CANCELLING IN THE 3RD MIXER OF THE FREQUENCY MULTIPLIER (Mc/s). AND IN THE 4TH MIXER OF THE FREQUENCY OFFSET UNIT.
2. FILTERS BETWEEN MIXER STAGES HAVE BEEN OMITTED FOR SIMPLICITY.

PRINCIPLE OF FREQUENCY OFFSETTING

FIG.10·1

| | | |

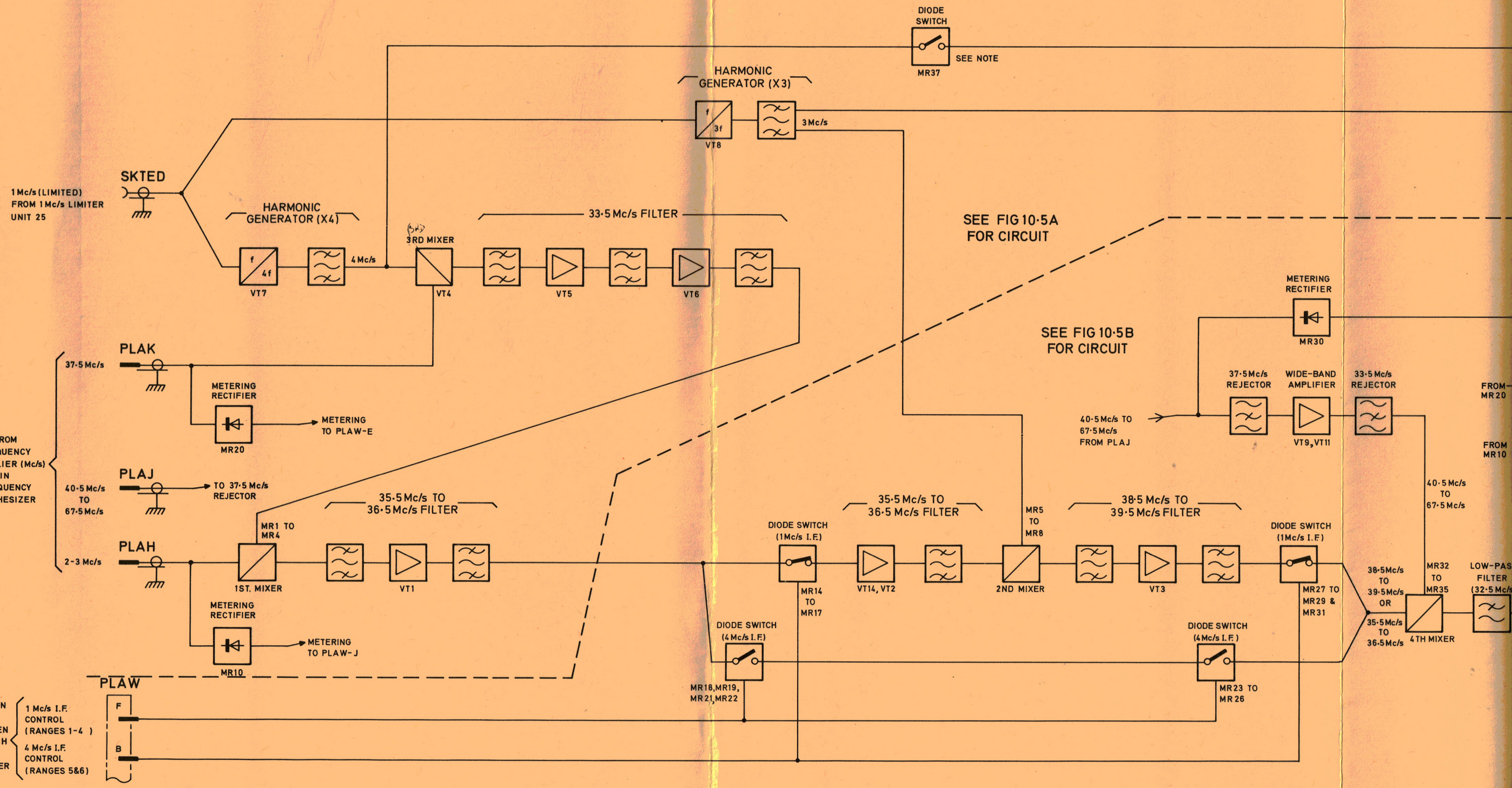


NOTE: DIODE SWITCH MR37 IS TURNED ON BY A SWITCHING CURRENT FROM THE METERING SWITCH 1SB2B (I.F. TEST ONDSB-4 Mc/s) VIA THE 4 Mc/s TEST SIGNAL SOCKET SKTET

FREQUENCY OFFSET UNIT 5820-99-519-7027

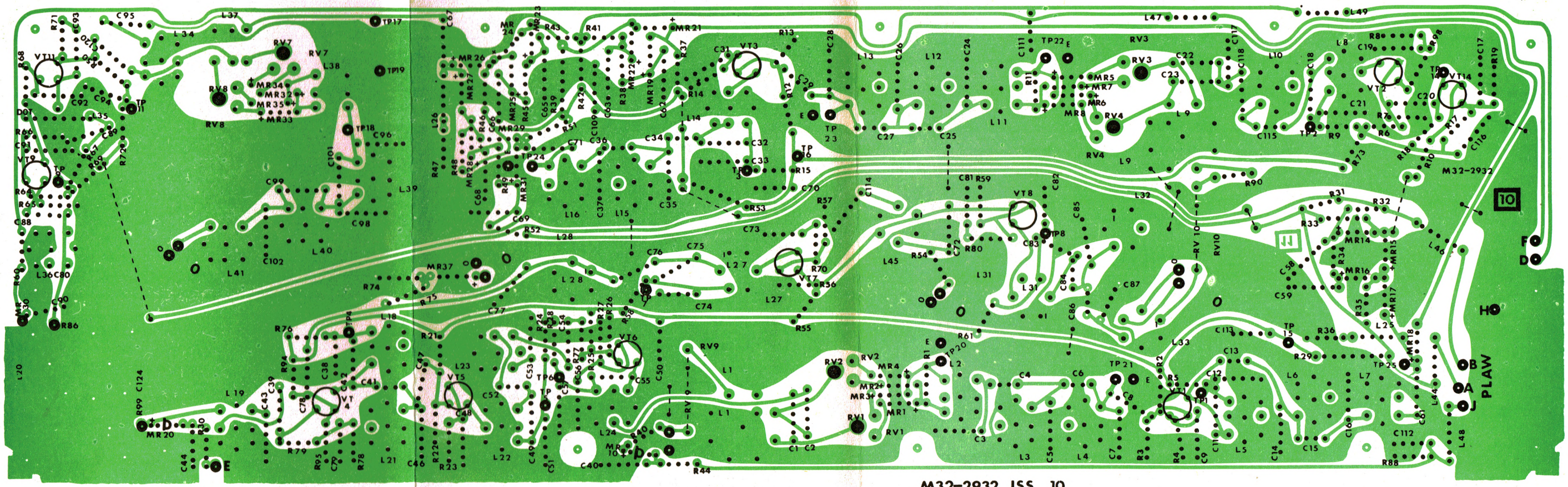
SUB-ASSEMBLY 3 BLOCK DIAGRAM

FIG.10·3



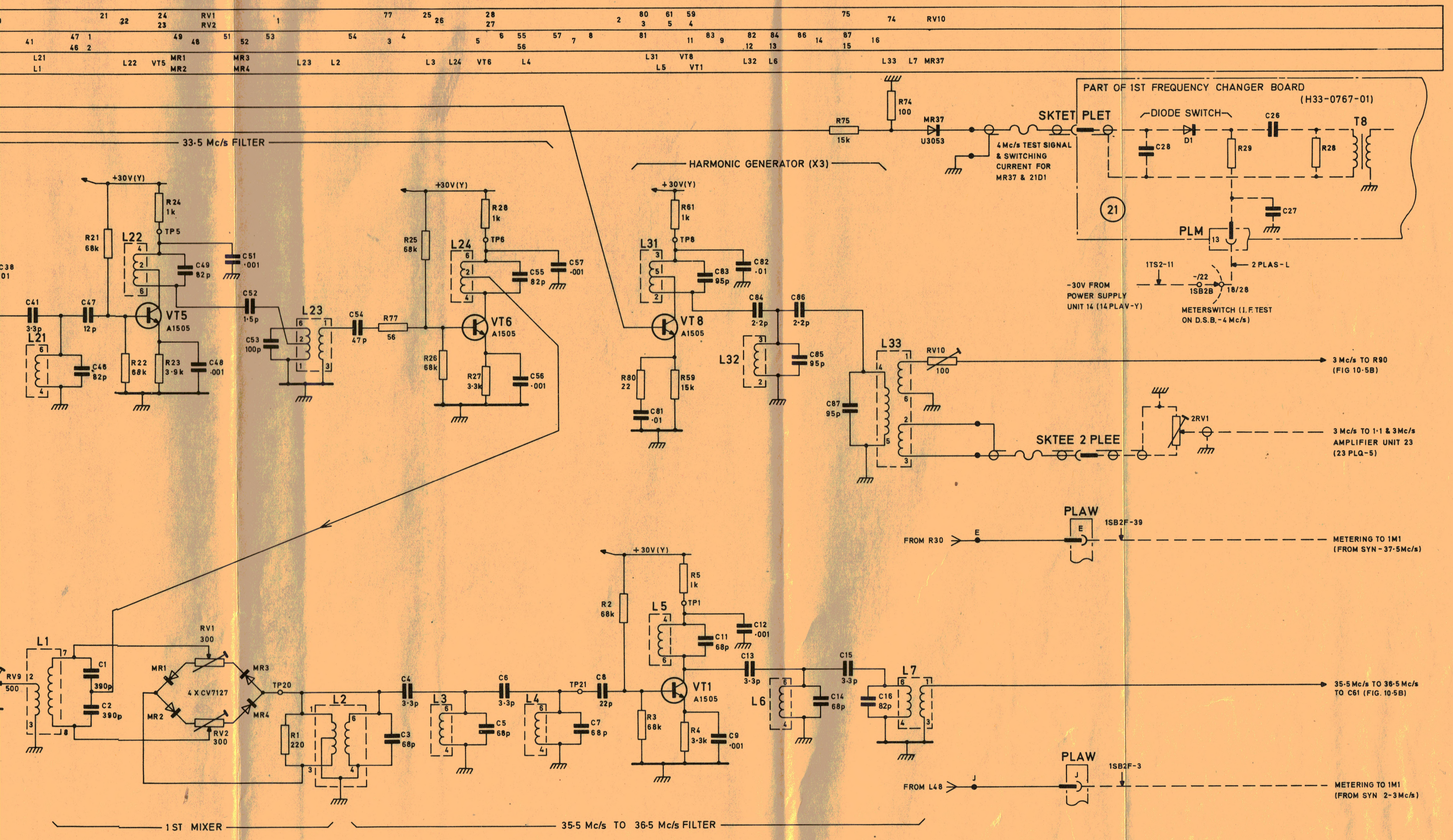
NOTE: DIODE SWITCH MR37 IS TURNED ON BY A SWITCHING CURRENT FROM THE METERING SWITCH 1SB2B (I.F. TEST ONDSB - 4 Mc/s) VIA THE 4 Mc/s TEST SIGNAL SOCKET SKTET

FREQUENCY OFF
SUB-ASSEMBLY 3



M32-2932 ISS 10

10.4 FREQUENCY OFFSET UNIT COMPONENT LAYOUT



NOTE: CANS OF ALL SCREENED INDUCTORS CONNECTED TO EARTH TRACK BY FIXINGS

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

FREQUENCY OFFSET UNIT 5820-99-519-7027

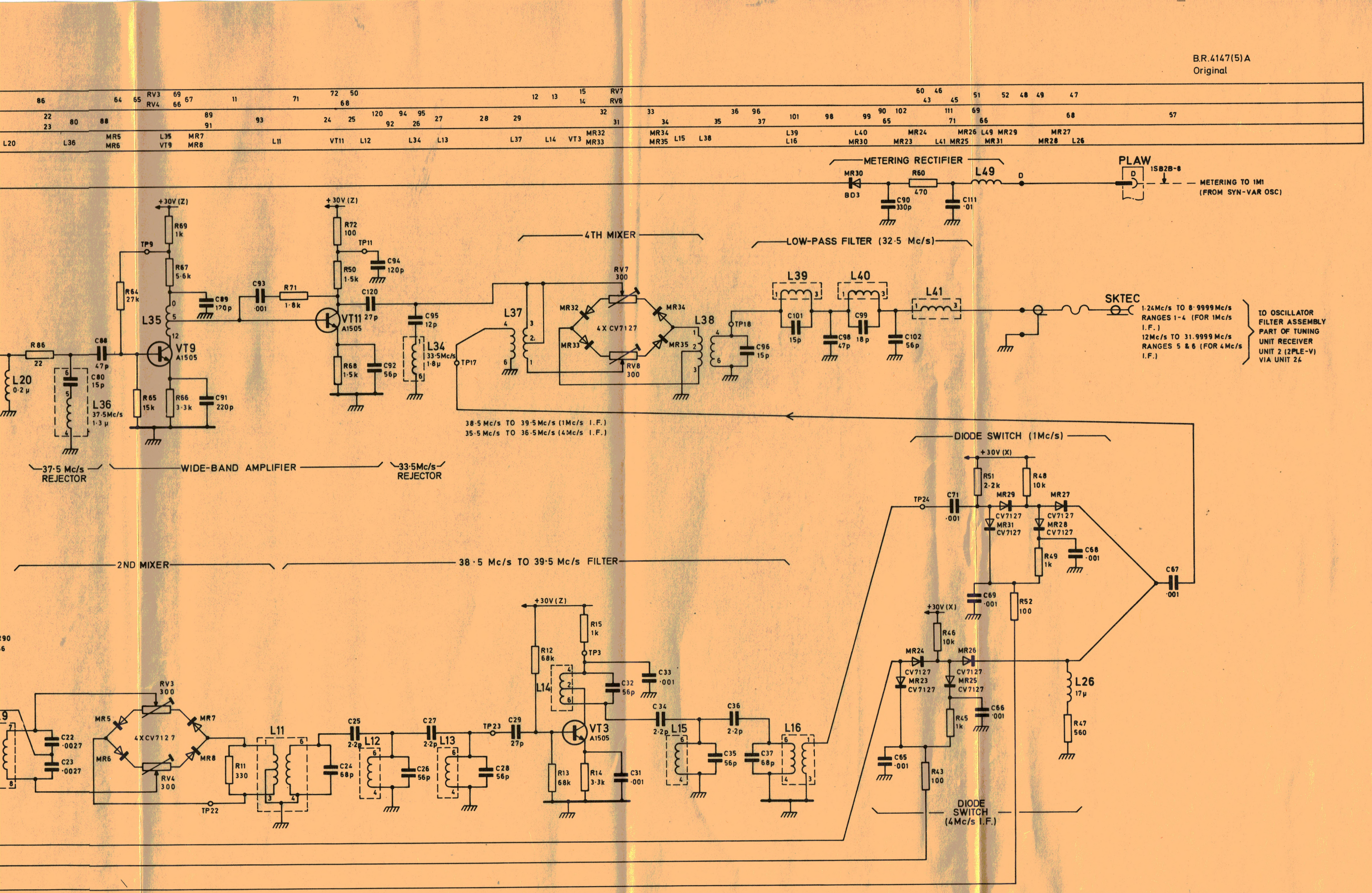
SUB ASSEMBLY 3

CIRCUIT DIAGRAM

FIG.10·5A

| | | |

B.R.4147(5)A
Original



NOTE CANS OF ALL SCREENED INDUCTORS CONNECTED TO EARTH TRACK BY FIXINGS

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

FREQUENCY OFFSET UNIT 5820-99-519-7027

SUB ASSEMBLY 3

CIRCUIT DIAGRAM

FIG.10·5B

| | | |